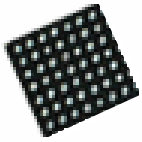
AV5205

24-bit, 102dB SNR audio DAC with supply modulation headphone amplifier

Features

- DAC
  - 102 dB SNR for the whole path
  - 5µVrms output noise (-6dB channel gain)
  - 24-bit audio DAC
  - Sampling rate: 8 kHz to 192 kHz
- Supply
  - Direct connection to the battery (2.3 V to 4.8 V)
  - Supply Modulation Audio Buffer (SMAB™) for headphone amplifier efficiency optimization
  - I/O supply: 1.62 V to 3.6 V
- Power consumption
  - Stand-by: 5 µWRev 1Playback consumption: 14 mW (no music), 17 mW with 50 mVrms signal, 31 mW with 300 mVrms signal
- Audio interface
  - I^2S input
  - Stereo single ended or differential analog input
- Clock
  - System clock input: 32 kHz, 13 MHz, 19.2 MHz, 26 MHz and 38.4 MHz
- Automatic startup sequence
- I²C control interface
- internal PLL generating audio clocks from 32 kHz



VFBGA-49 4x4x0.91mm 0.5mm pitch

- Analog output drivers
  - SMAB™ stereo headset amplifier
    - 'True ground' output amplifier (no coupling capacitor).
    - 2x17 mW on 32Ω or 16Ω
    - 84 dB programmable gain
    - Plug detection
    - True "pop and artefact free" thanks to internal start-up and shut down sequencing
  - Independent right & left channel control
  - Stereo differential line out

Description

The AV5205 is a 24-bit high performance DAC for mobile handset application.

The headphone amplifier is supplied with an embedded positive/negative DC-DC converter.

SMAB™ system scales the voltage of this positive/negative supply following the signal amplitude improving widely the amplifier efficiency.

The Pop noise canceller function consists of one state machine sequencing automatically the power-up/down of all blocks, plus an offset cancellation system attached to the output amplifier.These two systems allow to suppress all possible sources of audio transient artefact using a very simple register setting.

Embedded power management allows direct connection to the battery, reducing overall bill of material.

No additional quartz is required when the PLL is driven by the 32 kHz frequency.

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1 Overview

The AV5205 is designed to fit in most audio systems where high audio performance and long playback time are needed.

The AV5205 can work with optimal performance with a 32 kHz real time clock only. In addition, thanks to an integrated PLL, the AV5205 can provide system clock to the application allowing to turn off all other clock sources.

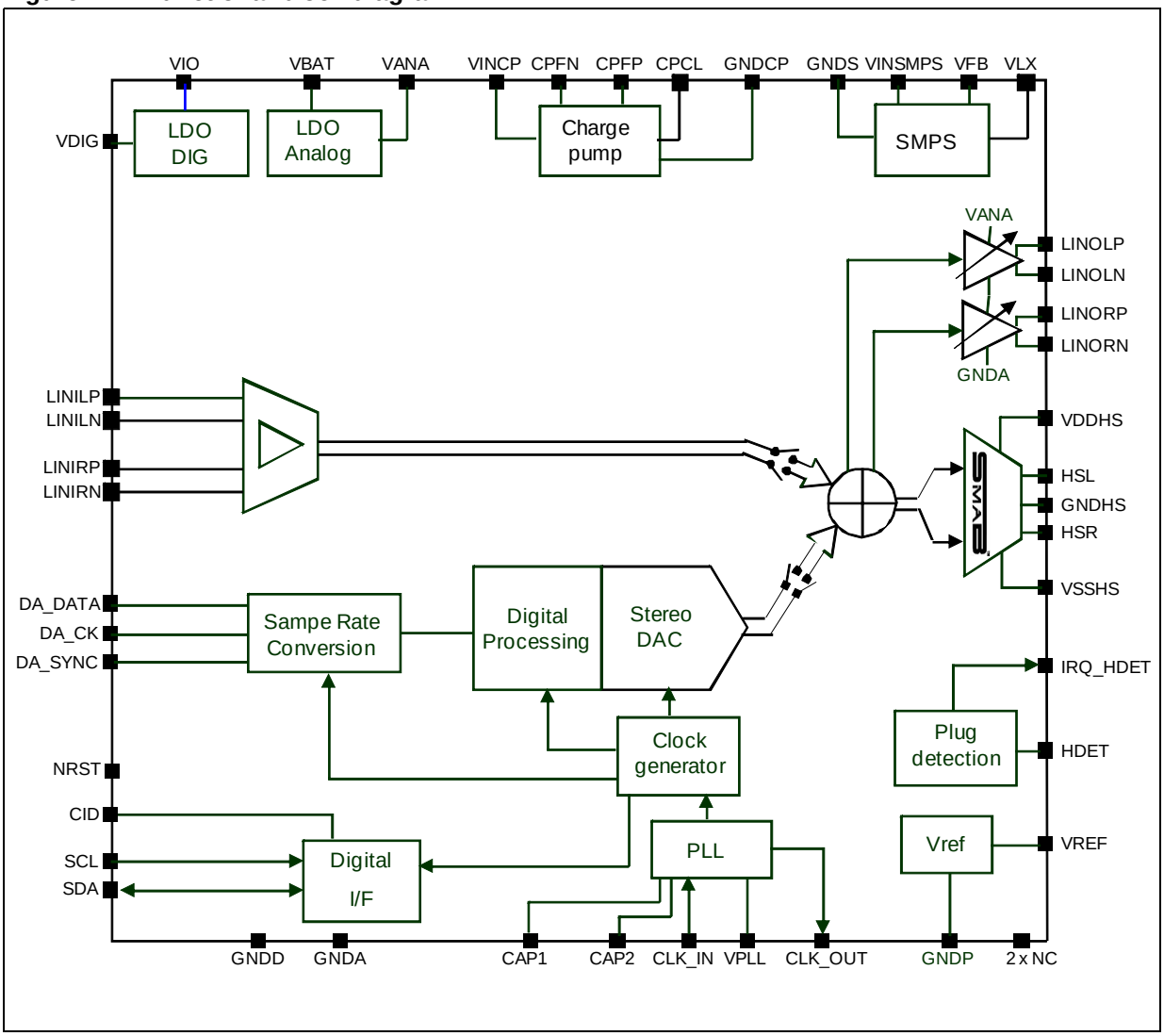
A sample rate converter then manages sampling rates from 8 kHz up to 192 kHz.

The headphone amplifier supply of the AV5205 is symmetrical, provided by a Switch Mode Power Supply (SMPS) for the positive side and a charge pump for the negative side. For the positive side, SMPS gives additional power efficiency improvement compared to a charge pump. The “Supply Modulation Audio Buffer” (SMAB™) allows to reach a good power efficiency whatever the audio signal amplitude is, keeping low harmonic distortion and noise floor.

The AV5205 control registers are accessed with an I²C compatible interface.

2 Functional block diagram

Figure 1. Functional block diagram



3 Pin description

Figure 2. Pin configuration (top view)

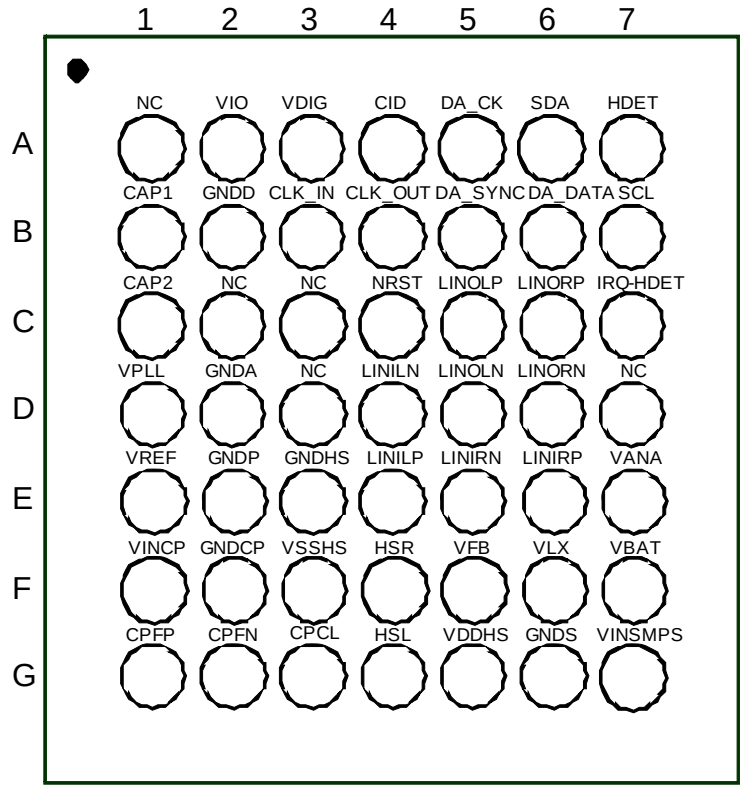


Table 1. Pin description

Pin number	Name	Type	Description
F7	VBAT	P	Positive power supply. Operating range 2.3 V to 4.8 V.
G7	VINSMPS	P	Positive power supply for SMPS. Operating range 2.3 V to 4.8 V
A2	VIO	P	Positive supply for IO's and digital. Operating range 1.62 V to 3.6 V
F1	VINCP	P	Positive supply for charge pump. Connected to VFB and VDDHS.
D1	VPLL	P	Positive supply for PLL
G6	GNDS	P	SMPS negative supply. 0 V
F2	GNDCP	P	Charge pump negative supply. 0 V
D2	GNDA	P	Analog negative supply. 0 V
B2	GNDD	P	Digital negative supply. 0 V
A3	VDIG	AO	Digital LDO output

Table 1. Pin description (continued)

Pin number	Name	Type	Description
E7	VANA	AO	Analog LDO output
F5	VFB	AIO	Feedback sensing for SMPS. To be connected to VDDHS
F6	VLX	AO	SMPS output. To be connected to 4.7µH coil
G5	VDDHS	AI	SMAB amplifier positive supply. To be connected to VFB
G1	CPCFP	AIO	Charge pump fly capacitor
G2	CPCFN	AIO	Charge pump fly capacitor
G3	CPCL	AO	Charge pump output
F3	VSSHS	AI	HS amplifier negative supply. To be connected to CPCL
E4	LINILP	AI	Line left channel positive input
D4	LINILN	AI	Line left channel negative input
E6	LINIRP	AI	Line right channel positive input
E5	LINIRN	AI	Line right channel negative input
C5	LINOLP	AO	Line left channel positive output
D5	LINOLN	AO	Line left channel negative output
C6	LINORP	AO	Line right channel positive output
D6	LINORN	AO	Line right channel negative output
G4	HSL	AO	Left output for headphone. Provides negative voltage down to -2 V. Common mode is 0 V
F4	HSR	AO	Right output for headphone. Provides negative voltage down to -2 V. Common mode is 0 V
E3	GNDHS	AI	Sense ground for headphone drivers. 0 V
A7	HDET	AI	Plug detection
B4	CLK_OUT	DO	Master clock output : 19.2 MHz to 78 MHz
B1	CAP1	AIO	Capacitor for VCO of the PLL
C1	CAP2	AIO	Capacitor for VCO of the PLL
B3	CLK_IN	DI	Master clock input. 32 kHz to 38.4 MHz.
C7	IRQ_HDET	DO	Plug detection interrupt request. Programmable open drain
E1	VREF	AIO	External decoupling for audio reference voltage
E2	GNDP	AIO	Ground for reference voltage
B7	SCL	DI	I²C clock
A6	SDA	DIO	I²C data
B6	DA_DATA	DI	I²S data
A5	DA_CK	DIO	I²S serial clock
B5	DA_SYNC	DIO	I²S frame sync
A4	CID	DI	I²C chip identification

Table 1. Pin description (continued)

Pin number	Name	Type	Description
C4	NRST	DI	Asynchronous reset
A1	NC	DI	For engineering purpose. Must be left unconnected
C2, C3, D3, D7	NC	-	Non connected

4 Functional description

4.1 General description

This product is optimized for:

- Very high audio quality
- Long audio playback time

AV5205 integrates:

- SMAB^{TM} amplifier for headphone amplifier efficiency optimization
- High dynamic range digital to analog converter
- 17 mW headphone driver
- Power management
  - One LDO for analog power supply
  - One LDO for the digital power supply
  - One charge pump for the headphone amplifier negative supply
  - One SMPS for the headphone amplifier positive supply and for the negative charge pump supply
  - One LDO for PLL
- One PLL

4.2 Audio quality improvement

Digital to analog converter performance:

- 24-bit stereo
- 102 dB dynamic range

The stereo headphone amplifier has real reference to ground (0 volts):

- No need for an external serial capacitor
- -80 dB to +4 dB programmable gain

4.3 Power management

The AV5205 includes 3 low-dropout linear regulators, a positive-negative switch mode power supply able to generate the supplies needed for its own operation:

- VDIG for digital section at 1.2 V nominal.
- VANA for analog section at 2.0 V nominal
- VPLL for PLL at 1.8V
- HS capless SMAB^{TM} amplifier supply:
  - VNCP for negative supply from -0.8 V to -1.7 V
  - VSMPS for positive supply from 1.2 V to 2.2 V

Control of SMAB^{TM} supply is done by the register.

These regulated voltages are not able to drive any other external load. The AV5205 performance is not guaranteed if these supplies are used for external components.

The VIO voltage must be provided from the system.

Warning: Although AV5205 features wide supply ranges for VBAT and VIO, VBAT must always be higher than VIO in order to avoid leakages and potential destruction of the circuit.

4.4 Clocking

System using AV5205 can be configured following 3 clock configurations:

1. Master clock is provided by the system clock connected to CLK_IN pin. System clock frequency can be 13 MHz, 19.2 MHz, 26 MHz or 38.4 MHz. The CLK_OUT output clock must be disabled in *Clock configuration register (address 17h)* register (default state). 32kHz clock is not needed in that configuration.
2. Master clock is provided to the system by the AV5205 from 32 kHz real time clock through CLK_OUT pin. Master clock provided to the system can be 19.2 MHz, 26 MHz, 38.4 MHz, 52 MHz, 76.8 MHz or 78 MHz. This mode allows to power down modem clock which is generally much more consuming than this embedded PLL. The CLK_OUT output clock frequency must be configured in *Clock configuration register (address 17h)* register.
3. AV5205 uses the 32 kHz real time clock but does not provide master clock to the system. The CLK_OUT output clock must be disabled in *Clock configuration register (address 17h)* register (default state). Only 32 kHz real time clock is needed for the AV5205.

4.5 Wake up

The wake-up mechanism involves battery and IO voltage management. Once VBAT power is on and VIO voltage valid, the AV5205 can be reset by the NRST pin.

Figure 3 describes the wake-up and stop sequence.

4.6 “Pop and click” noise cancellation

AV5205 includes a set of features ensuring audio artefact removal. These artefacts or audible effects, commonly named “pop and click” noise, are naturally generated when amplifiers are powered up, when audio switches configuration is changing or when gain is changed. All these potential audio artefact sources are managed inside the AV5205 with “anti-click” and “Pop Smooth Machine (PSM)”.

4.6.1 Fade in, fade out

Fade in and fade out allow to operate a smooth step by step transition on gains when changing from one value to another. The time to change from one gain step to another must be set in *Fade in (address 1Ch)* register according the desired audio effect.

Fade in can be bypassed in *Fade in (address 1Ch)* register if not needed.

Fade out is always active when audio channel is powered down through register.

4.6.2 Pop Smooth Machine (PSM)

AV5205 includes a sequencer (PSM) that reduces drastically software driver complexity. In addition, it sequences the power up and power down of the different blocks of the audio channel in order to avoid any audio artefact like “pop noise”.

All actions relative to PSM are included in the register. The PSM is launched automatically after register writing. The end of the sequence can be checked interrupt on IRQ_HDET output if the interrupt is unmasked in the *Interrupt mask control (address 12h)* register. The polarity of this interrupt signal and open-drain control are also programmable by the *Interrupt polarity control (address 10h)* and *Interrupt open drain control (address 11h)* registers. The *PSM_END* bit of the *Interrupt status (address 13h)* register is then set, and is automatically reset after reading. The IRQ_HDET output is reset after reading the *Interrupt status (address 13h)* register.

ISEL and *OSEL* bits in register allows to enable respectively the input (DAC or line in) and the output (headphone or line out driver). Once written, the PSM is launched and the audio path is set according the inputs/outputs selection.

To set a new *ISEL*, *OSEL* configuration (change input/output or shut-down), it is needed that PSM cycle has finished.

 register must be written after digital interface, data transfer mode, interrupt and master clock setting for power up (see *Figure 3*).

Figure 3. Wake up sequence

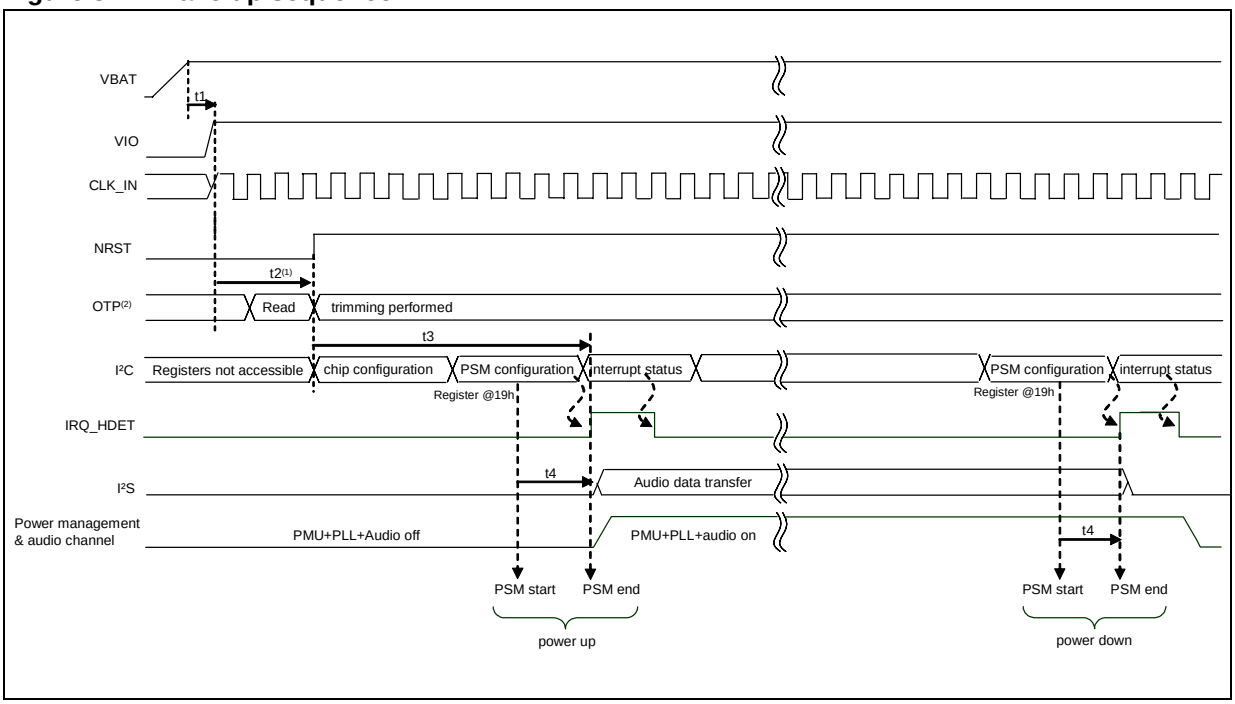


Table 2. Wake up timings

Symbol	Parameter	Min.	Max.	Unit
t1	Delay of VIO rising from VBAT valid	500		µs
t2[1]	Chip auto-trimming through OTP[2] reading		5	ms
t3	chip configuration using sequence described in *4.6.3* (fade in not included, I²C frequency 400 kHz)		2	ms
t4	PSM delay		10	ms

1. t2 occurs only once when VIO voltage is rising. This sequence is not done for the following power-up if VIO is kept
2. OTP stands for One Time Programmable memory used to trim electrical parameters inside the chip

4.6.3 Start-up and stop sequences

1. Start-up:
   - I2C setting + digital interface configuration: @04h, @05h
   - Clock configuration, audio sample rate: @07h, @17h
   - Data transfer mode (Data transfer enabled): @06h
   - Gain configuration (line in, DAC, line out, headphone): @08h -> @0Fh
   - Interrupt configuration: @10h -> @12h
   - Headphone load model, Vbat min.: @18h
   - HS configuration (threshold, enable): @1Ah
   - Fade-in bypass configuration: @1Ch
   - ISEL, OSEL configuration (audio path selection): @19h

2. Stop sequence:
   - ISEL, OSEL configuration (audio path disabled): @19h
   - Soft reset: @18h

4.7 Audio playback data transfer

A sample rate converter allows fully asynchronous transfer from the modem or audio processor to the AV5205. 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 96 and 192 kHz sampling rates are supported. PLL can be bypassed and shut down to save power consumption if CLK_IN frequency is 19.2 MHz[a], 26 MHz or 38.4 MHz. PLL must be powered up if CLK_IN frequency is 13 MHz.

CLK_OUT can be configured to provide master clock to the system: 19.2 MHz, 26 MHz, 38.4 MHz, 52 MHz, 76.8 MHz or 78 MHz are supported.

The *CLK_IN_FREQ* and *SRATE* sections of the *Audio mode (address 07h)* register must be written to give the AV5205 the information for its internal clock system management. The jitter and spectral properties of the system master clock have a direct impact on the DAC performance.

a. For 192kHz sample rate with CLK_IN=19.2MHz, PLL must be on

4.8 Supply modulation

AV5205 includes SMAB^{TM}. This system performs an envelope detection on the audio signal and adapts the positive and negative supplies of the headphone amplifier to the minimum value needed by the amplifier to ensure good audio quality, suppressing un-needed drop-out losses commonly affecting AB class amplifiers.

The headphone amplifier supply takes two values depending on the envelope detection level. This detection level can be programmed to find the better compromise between power efficiency and audio performance for the whole system, including the headphone.

The detection level can be set from 0% to 100% of the DAC signal full dynamic (0dBFS) in the register. 0% means supply is always at high level, 100% means supply is always at low level whatever the audio signal is. The SMAB^{TM} threshold integrates the channel gain programming (digital and analog), allowing to adapt headphone supply to the true audio output signal level (there is no need to change threshold value in the register if gain is changed).

The threshold level is set with the *SMAB_THRESHOLD[6:0]* bits following the formula:

SMAB^{TM} threshold = 2^{BDEPTH}. **SMAB_THRESHOLD**[6:0]

Default state is **SMAB_THRESHOLD**[6:0] = ‘100000’ corresponding to 32% or +/-452mV, corresponding to 320mVrms output signal when channel gain is 0dB.

For example:

SMAB_THRESHOLD[6:0] is set to ‘101000’ (40 in decimal, 40% of the full scale digital input signal)

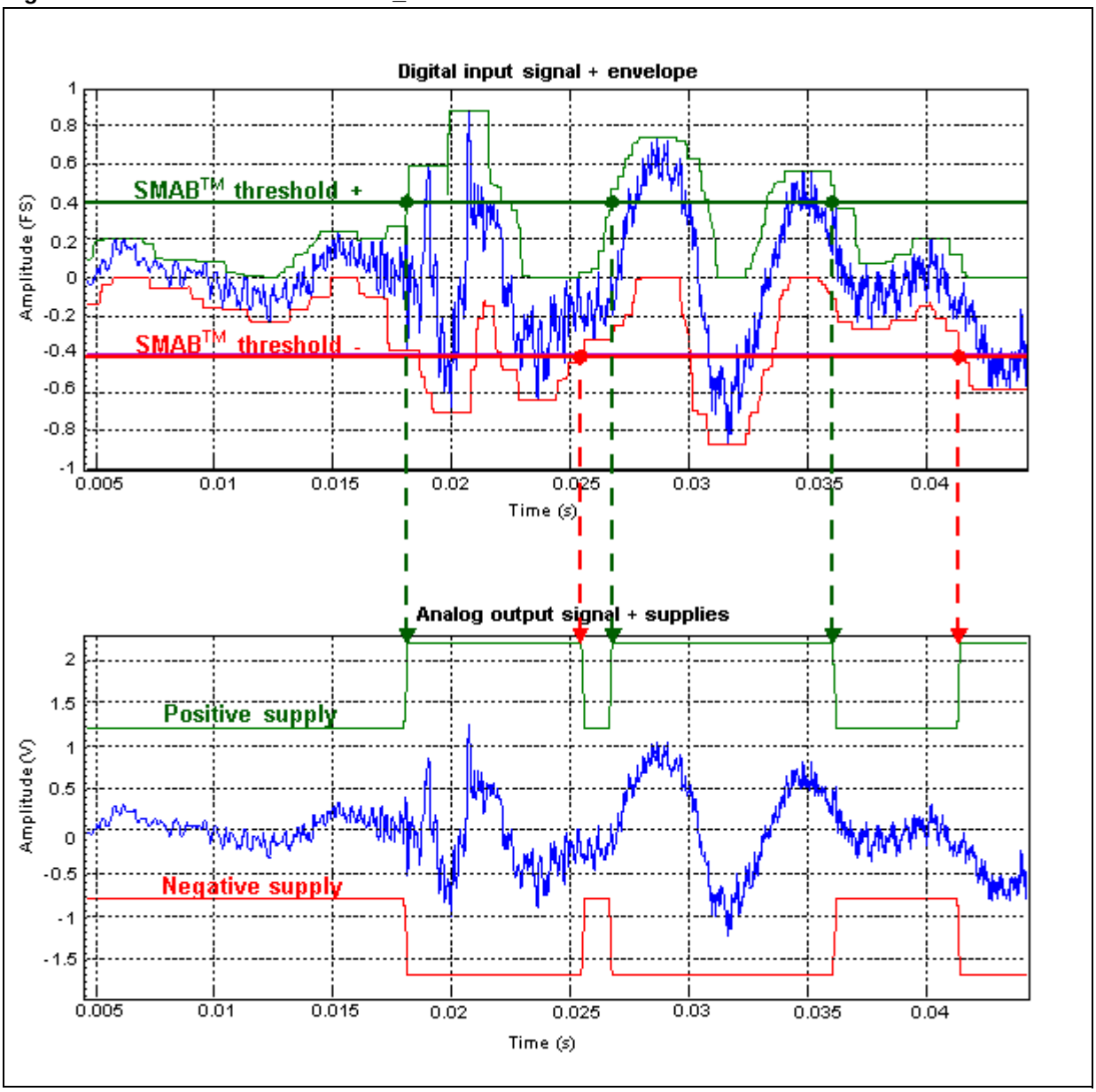
BDEPTH[1:0] is set to ‘01’ (24 bits words)

HSGL[1:0] is set to ‘110’ (0dB gain on headset amplifier)

DACGL[5:0] is set to ‘111101’ (0dB on DAC gain)

SMAB^{TM} threshold = +/-3355443 in decimal (40% of the full scale digital input signal), corresponding to +/-566mV or 400mVrms output signal (see *Figure 4*).

Figure 4. Waveforms with SMAB_THRESHOLD=28h



An attack and decay time is added to the envelope signal to build the supply modulation signal. This prevents fast switching of the switch mode power supply from one state to another, avoiding power losses and audible artefacts. An ‘or’ mask is used between positive and negative envelope of the left and right channel to produce the supply modulation signal for the stereo path.

4.9 Control registers

The AV5205 internal control registers are accessed through the I²C interface.

Refer to *Section 6* for register descriptions.

4.10 Audio digital interface

Audio digital interface is I²S like. the interface can have different rates and can work in different formats and modes. It can operate in Slave or Master mode

The pins used by the interfaces are: DA_SYNC, DA_CK and DA_DATA word clock, bit clock and data, respectively.

Data is exchanged with left channel data first in all formats. Channel order (left/right) can be switched with bit *DACHSW*.

4.10.1 Master mode

When Master mode is selected (bit *DAMAST* set) the DA_SYNC and DA_CK clocks are generated internally, and are provided to the external pads (DA_CK and DA_SYNC are outputs). The DA_SYNC frequency is generated by the internal clock system. DA_CK is equally spaced within the DA_SYNC frame. The number of bit clock in each I2S word is programmed by the bit *FLENGTH* in register *Digital audio interface configuration 2 (address 05h)*.

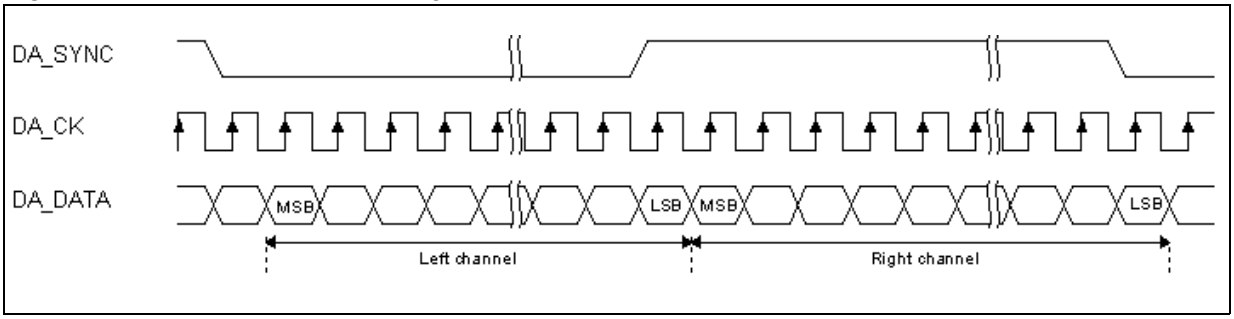
It delivers the number of cycles corresponding to the word length programmed in the *Digital audio interface configuration 1 (address 04h)* register. DA_CK is generated by a fractional divider which produces cycle-to-cycle jitter below 40 ns.

Table 48 shows the true DA_SYNC and DA_CK frequencies for the different master clock frequencies in master mode.

4.10.2 Supported operating formats

Delayed format (I²S compatible) (*DAFORM* = 00): the audio interface is I²S compatible (see *Figure 5*). The number of CK periods within one SYNC period is not relevant, as long as enough CK periods are used to transfer the data and the maximum frequency limit specified for bit clock is not exceeded. CK can be either a continuous clock or a sequence of bursts. Bits *DASYNC* and *DACKP* affect the interface format inverting the polarity of DA_SYNC and DA_CK pins respectively.

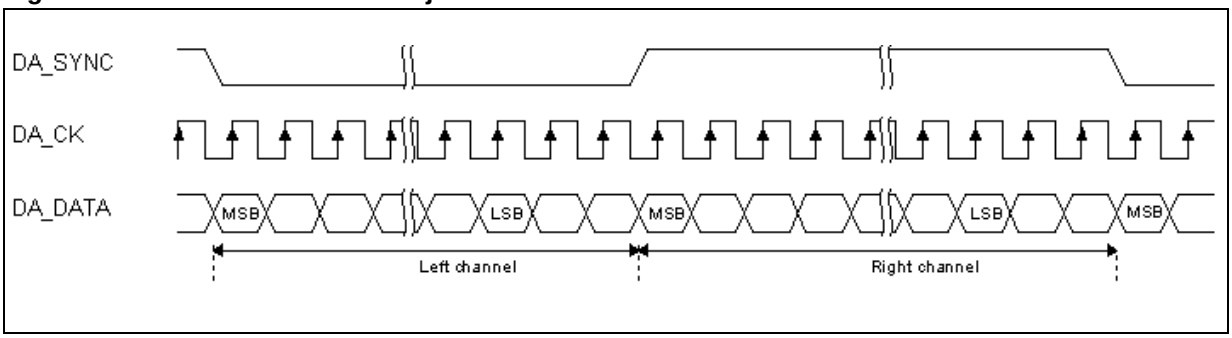
Figure 5. Audio interfaces: delayed format



The LSB satisfies the general I²S data property. It is ignored if the programmed word size is smaller than the word size of the audio processor, and it is '0' padded if the programmed word size is greater than the word size of audio processor.

Left-aligned format (*DAFORM* = 01): this format is equivalent to delayed format without the 1 bit clock delay at the beginning of each frame (see *Figure 6*). Data is exchanged with MSB first (*ENDIAN* = 0) or LSB first (*ENDIAN* = 1).

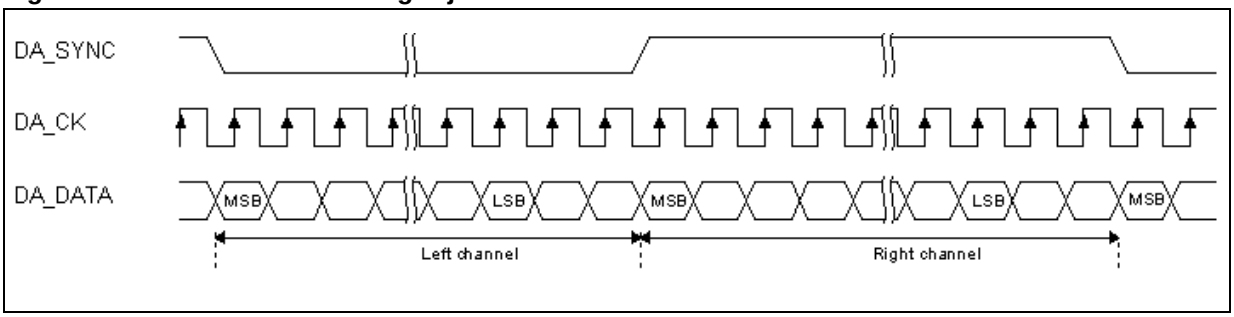
Figure 6. Audio interfaces: left justified format



The left-justified format is not strictly I²S compatible. The MSB (or LSB respectively) is sent just after the falling edge of the synchronization signal. Bits after the LSB (or MSB respectively) are ignored.

Right-aligned format (*DAFORM* = 10): this format is equivalent to delayed format, except that the audio data are right aligned (see *Figure 7*). Data is exchanged with MSB first (*ENDIAN* = 0) or LSB first (*ENDIAN* = 1).

Figure 7. Audio interfaces: right-justified format



The right-justified format is not strictly I²S compatible. The LSB (or MSB respectively) is sent just before the rising edge of the synchronization signal. Bits before the MSB (or LSB respectively) are ignored.

For left and right justified format, I²S frame length has to be programmed by the *FLENGTH* section of the *Digital audio interface configuration 2 (address 05h)* register. It can be programmed as 2 x 32 bits, 2 x 24 bits or 2 x 16 bits.

Timings

Figure 8. Audio interface timing: master mode

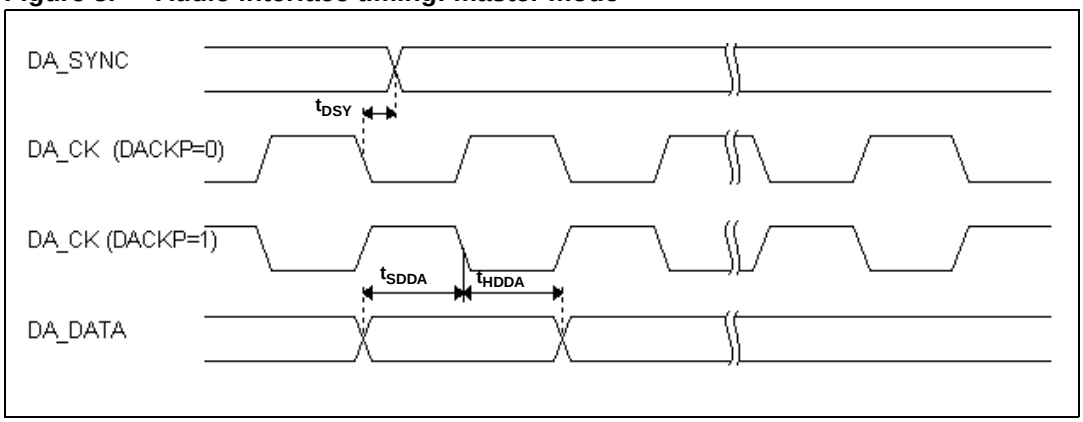


Figure 9. Audio interface timing: slave mode

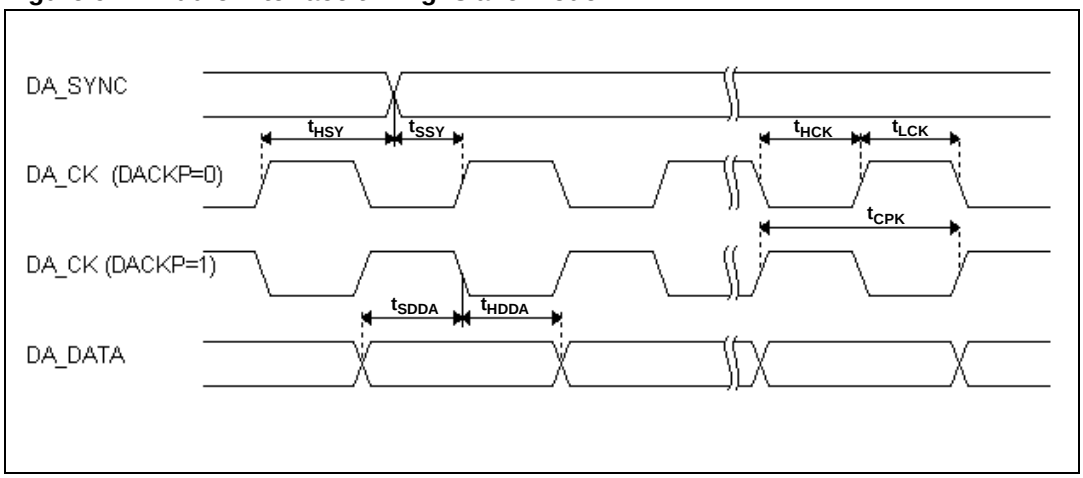


Table 3. Audio interface I²S timings

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{DSY}	Delay of DA_SYNC edge from DA_CK active edge	Master mode	-	-	0.8* t_{PCK}	ns
t_{SDDA}	Setup time DA_DATA to DA_CK active edge	-	5	-	-	ns
t_{HDDA}	Hold time DA_DATA from DA_CK active edge	-	4	-	-	ns
t_{SSY}	Setup time DA_SYNC to DA_CK active edge	Slave mode	0.2* t_{PCK}	-	-	ns
t_{HSY}	Hold time DA_SYNC from DA_CK active edge	Slave mode	5	-	-	ns
t_{PCK}	Period of DA_CK	Slave mode	20	-	-	ns
t_{HCK}	DA_CK pulse width high measured from VIH to VIH	-	0.35* t_{PCK}	-	-	ns
t_{LCK}	DA_CK pulse width low measured from VIL to VIL	-	0.35* t_{PCK}	-	-	ns

4.11 Control interface

The AV5205 control interface is a standard I²C interface described in the I²C specification of Philips Semiconductor version 2.1 of January 2000:

- A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START (S) condition.
- A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP (P) condition.

S and P conditions are always generated by the master.

- START (S) and repeated START (Sr) conditions are functionally identical. In this document, S is used for S or Sr conditions.
- Data is transmitted MSB first
- Acknowledge is a zero data line pull down done by the slave
- Not Acknowledge is a high-impedance data line done by the slave

The control interface supports both standard mode (100 kHz) and fast mode (400 kHz).

The device address can be changed with the CID pin connection:

CID tied to ground: chip address is **00111000(38h)** for writing, **00111001(39h)** for reading

CID tied to VIO: chip address is **00111010(3Ah)** for writing, **00111011(3Bh)** for reading

Figure 10. Control interface I²C format

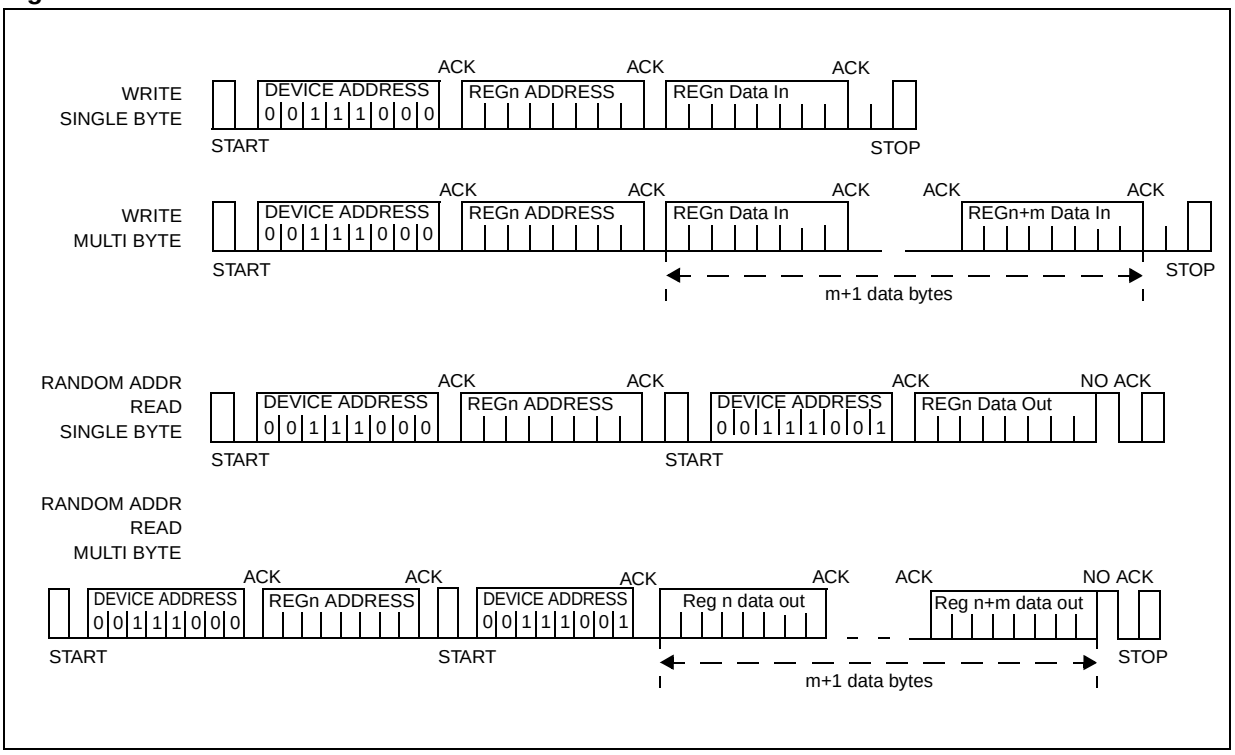


Figure 11. Control interface I²C format timing

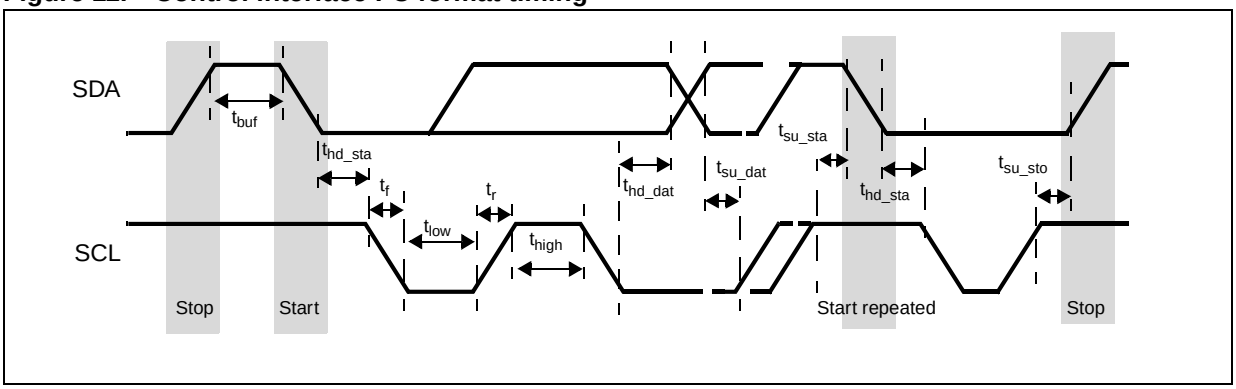


Table 4. Control interface I²C timings for standard mode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Clock frequency	-	-	-	100	kHz
t_{HIGH}	Clock pulse width high	-	600	-	-	ns
t_{LOW}	Clock pulse width low	-	1300	-	-	ns
t_R	SDA and SCL rise time	From 30% to 70%	-	-	1000	ns
t_F	SDA and SCL fall time	From 30% to 70%	-	-	300	ns
$t_{HD:STA}$	Start condition hold time	-	4000	-	-	ns
$t_{SU:STA}$	Start condition setup time	-	4000	-	-	ns
$t_{HD:DAT}$	Data input hold time	-	5	-	-	ns
$t_{SU:DAT}$	Data input setup time	-	4000	-	-	ns
$t_{SU:STO}$	Stop condition setup time	-	600	-	-	ns
t_{BUF}	Bus free time	-	4700	-	-	ns

Table 5. Control interface I²C timings for fast mode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Clock frequency	-	-	-	400	kHz
t_{HIGH}	Clock pulse width high	-	600	-	-	ns
t_{LOW}	Clock pulse width low	-	1300	-		ns
t_R	SDA and SCL rise time	From 30% to 70%	20+0.1*Cb(1)	-	1000	ns
t_F	SDA and SCL fall time	From 30% to 70%	20+0.1*Cb	-	300	ns
$t_{HD:STA}$	Start condition hold time	-	600	-	-	ns
$t_{SU:STA}$	Start condition setup time	-	600	-	-	ns
$t_{HD:DAT}$	Data input hold time	-	5	-	-	ns
$t_{SU:DAT}$	Data input setup time	-	250	-	-	ns
$t_{SU:STO}$	Stop condition setup time	-	600	-	-	ns
t_{BUF}	Bus free time	-	1300	-	-	ns

1. C_b = total capacitance of one bus line in pF.

4.12 Analog inputs: LINE IN

The AV5205 has a stereo line single-ended or differential input amplifier. If single-ended inputs are used, the complementary input must be grounded through a 100 nF capacitor (*Figure 15*). The input gain is in the range -42 dB up to 20 dB. The Line-In amplifier gains are controlled by the *Line in left configuration (address 08h)* and registers. If balance is enabled in *Balance configuration (address 16h)*, left channel gain setting is duplicated on right channel.

4.13 Analog outputs

4.13.1 Headphone output

The AV5205 provides a stereo single ended output referred to real ground (0 V) supplied from the negative side by a negative charge pump.

This headphone driver is intended to feed a headphone with 16 Ω load minimum impedance. To ensure amplifier stability with any headphone, a serial resistor plus a parallel capacitor must be placed before the load (see *Table* for components value). The output gain is regulated in the -18 to +2 dB range. Additional gain range is provided by the digital gain from -62 to 2 dB which provides a -80 to +4 dB overall gain range.

The stereo headphone amplifier gains are controlled by the *Headset left output configuration (address 0Ah)* and registers. If balance is enabled in *Balance configuration (address 16h)*, left channel gain setting is duplicated on right channel.

4.13.2 Line output

A stereo differential output is able to drive an external loudspeaker amplifier with a programmable gain from -30 dB to 0 dB by 3 dB steps. The line-output amplifier gains are controlled by the *Line out left configuration (address 0Eh)* and *Line out right configuration (address 0Fh)* registers. If balance is enabled in *Balance configuration (address 16h)*, left channel gain setting is duplicated on right channel.

4.14 DAC path

The DAC path converts digital data from the audio interface to analog domain and feeds it to the headphone and line-out amplifier.

The DAC path includes a digital gain control in the range of -62 to 2 dB. The DAC gain is controlled by the *DAC left configuration (address 0Ch)* and registers. If balance is enabled in *Balance configuration (address 16h)*, left channel gain setting is duplicated on right channel.

When AV5205 uses the 32 kHz real time clock, the jitter could impact the audio performance (dynamic range and SNR). Refer to *Figure 17*.

4.15 Gain programming

There are two programing modes for gain, depending on the configuration of the *Balance configuration (address 16h)* register.

In the default state, the left register drives both left and right paths in terms of gain.

When the balance bit is set for one block, left and right channel programming are independent in terms of gain.

Swapping from one mode to another does not change the left or right path. Only a register update changes the state effectively.

4.16 Mixing

It is possible to mix analog line input with the DAC path. Channel mixing is controlled by the *ISEL* and *OSEL* bits in registers. If both DAC and LINE IN are enabled, they are mixed together.

4.17 PLL

A low jitter PLL is used to generate internal clock and/or external clock for the platform. PLL is activated automatically by PSM once *ISEL* and *OSEL* bits in registers are set (see *Section 4.6: "Pop and click" noise cancellation*).

The PLL is activated only if it is required by the channel configuration. For instance, if Line in to Line out path is selected, the PLL is powered down.

4.18 Analog-only operation

When pure analog path is selected (Line in to Line out or Line in to HS) the PLL is powered down automatically after *ISEL* and *OSEL* bits in register.

4.19 Plug detection

The AV5205 can detect the plug-in or plug-out of a headphone connector through a switch that grounds the HDET input when the plug is inserted.

A pull-up resistor to VIO must be placed on the HDET line (see *Figure 13* and *Figure 14* for application schematics). If plug detection is not used, HDET pin must be grounded and interrupt masked in *Interrupt status (address 13h)*.

When the HDET input is low (below 0.9 V), an interrupt signal is sent at the IRQ_HDET output if the interrupt is unmasked in the *Interrupt mask control (address 12h)* register. The polarity of this interrupt signal and open-drain control are also programmable by the *Interrupt polarity control (address 10h)* and *Interrupt open drain control (address 11h)* registers. The *HDET* bit of the *Interrupt status (address 13h)* register is then set, and is automatically reset after reading. The IRQ_DET output is reset after reading.

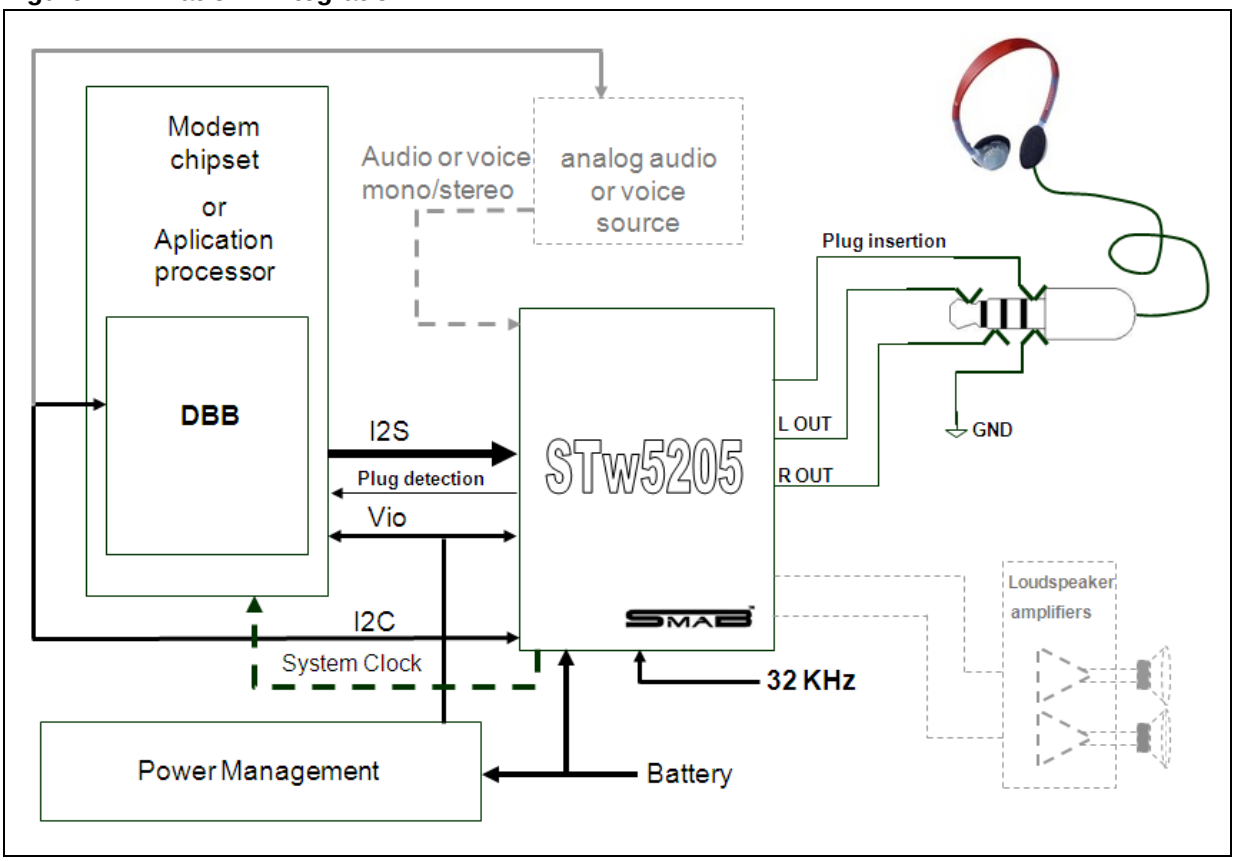
In the same way, an unplug generates an interrupt on the IRQ_DET pin provided the interrupt has been reset by a previous read. The *HEADSET* bit of *Chip status (address 14h)* registers gives the information if headset is connected or not.

5 Application information

5.1 Platform integration

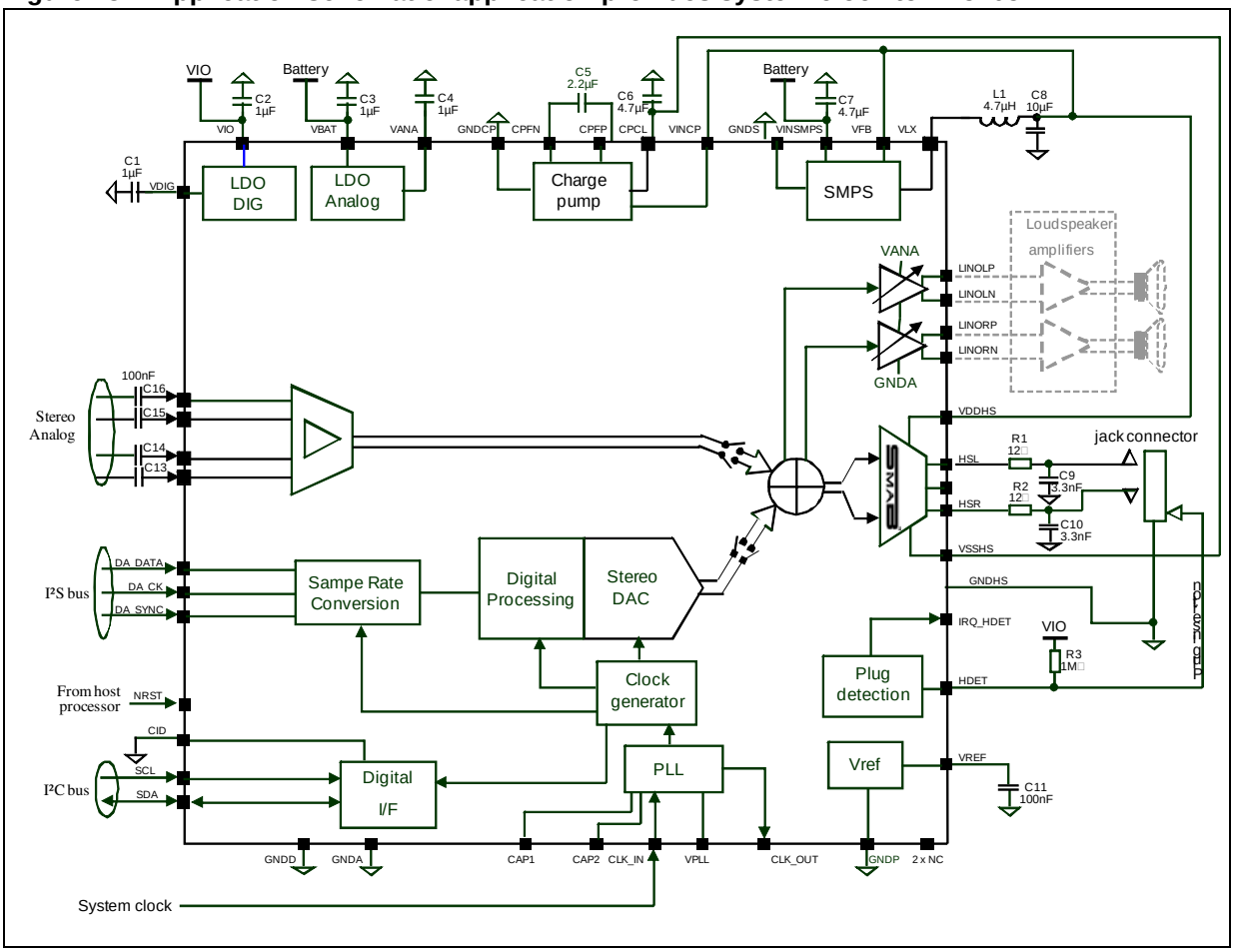
The AV5205 device has enhanced audio quality and playback duration. An example of easy integration is shown in *Figure 12*.

Figure 12. Platform integration



5.2 Application schematic

Figure 13. Application schematic: application provides system clock to AV5205



Note: Capacitors connected to CPCF1, CPCF2, CPCL and VINSMPS pins must be routed as close as possible from the chip.

Table 6. List of material when master clock is provided to AV5205

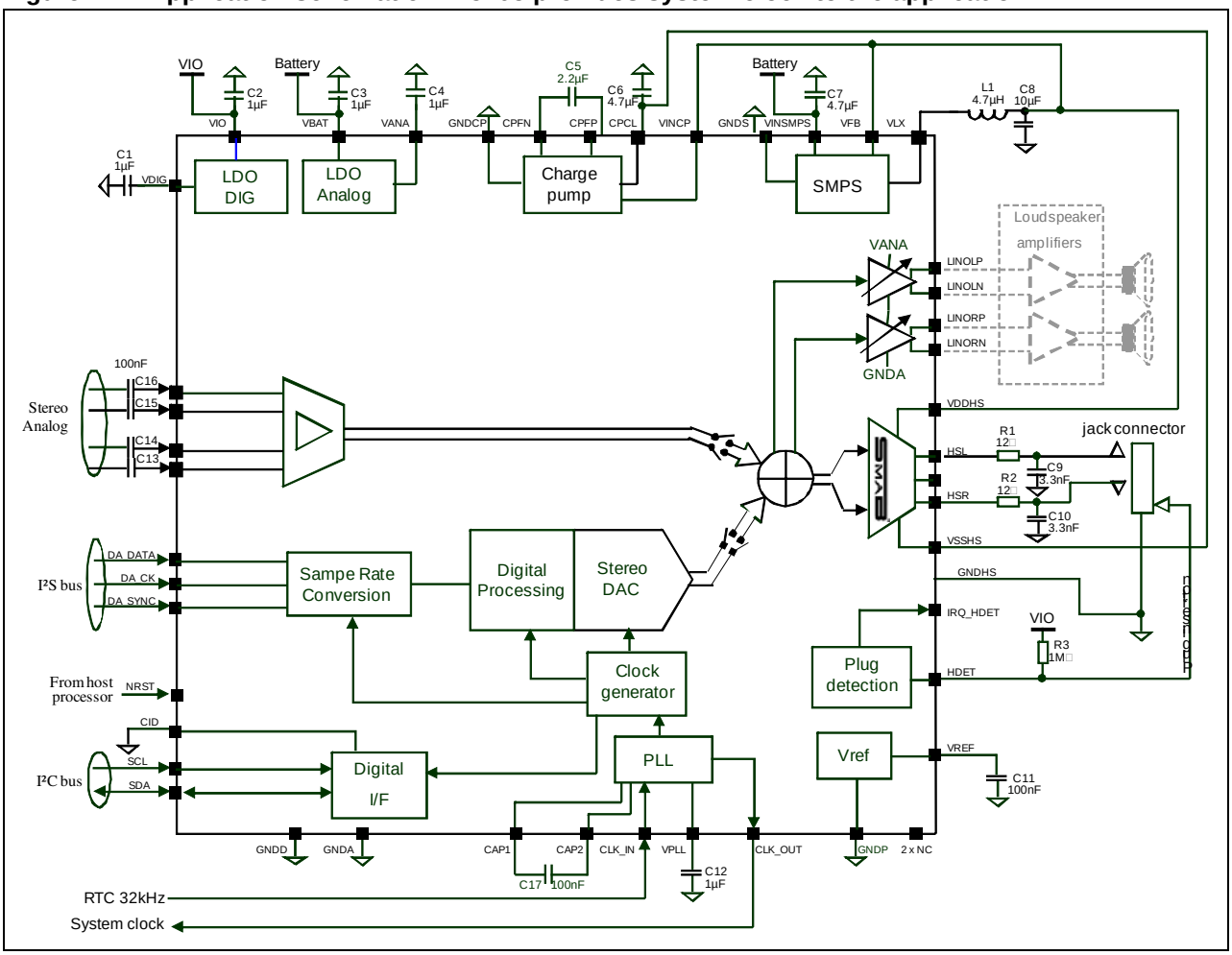
Name	Min	Nominal	Max	Unit	Code order	Provider
C8	4.1	10		µF	(CC0603) C1608X5R0J106M	TDK
C6, C7	1.3	4.7		µF	(CC0603) C1608X5R0J475M	TDK
C5	0.9(1)	2.2	2.7	µF	(CC0603) C1608X5R0J225K	TDK
C1, C2, C3, C4	0.4	1	2.7	µF	(CC0402) C1005X5R0J105K	TDK
C11,C13, C14, C15, C16		100		nF	(CC0402) C1005X5R0J104K	TDK
C9, C10		3.3nF			(CC0201) C0603X5R1E332K	TDK
R1,R2	12	-	-	Ω	-	-

Table 6. List of material when master clock is provided to AV5205 (continued)

Name	Min	Nominal	Max	Unit	Code order	Provider
R3		1		MΩ	-	-
L1	3.3	4.7	6.1	µH	MIPSZ2012D4R7	FDK

1. Including DC bias drift, temperature and aging

Figure 14. Application schematic: AV5205 provides system clock to the application



Note: Capacitors connected to CPCF1, CPCF2, CPCL and VINSMPS pins must be routed as close as possible from the chip.

Table 7. List of material when master clock is provided by AV5205

Name	Min	Nominal	Max	Unit	Code order	Provider
C8	4.1	10		µF	(CC0603) C1608X5R0J106M	TDK
C6, C7	1.3	4.7		µF	(CC0603) C1608X5R0J475M	TDK
C5	0.9(1)	2.2	2.7	µF	(CC0603) C1608X5R0J225K	TDK

Table 7. List of material when master clock is provided by AV5205 (continued)

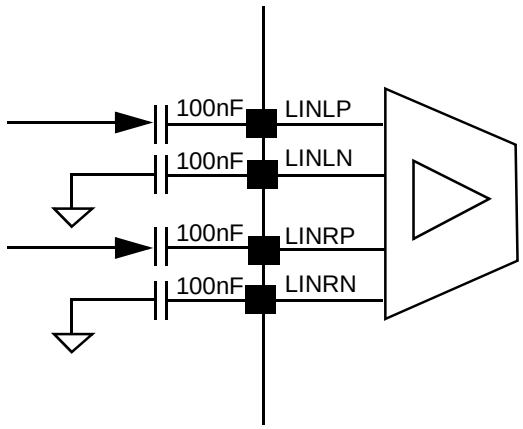
Name	Min	Nominal	Max	Unit	Code order	Provider
C1, C2, C3, C4, C12	0.4	1	2.7	µF	(CC0402) C1005X5R0J105K	TDK
C11, C13, C14, C15, C16, C17		100		nF	(CC0402) C1005X5R0J104K	TDK
C9, C10		3.3nF			(CC0201) C0603X5R1E332K	TDK
R1,R2	12	-	-	Ω	-	-
R3		1		MΩ	-	-
L1	3.3	4.7	6.1	µH	MIPSZ2012D4R7	FDK

1. Including DC bias drift, temperature and aging

5.3 Line in connection

Line in amplifier can be used in single ended. In that configuration, unused inputs must be grounded through 100nF capacitors.

Figure 15. Line in single ended application schematic



6 Register map

Table 8. Register map

Register set	Field name	Size (bits)	Register address (8 bits)	Access	Reference
Chip ID	Vendor ID Low	8	00h	Rd	*Table 9*
	Vendor ID High	8	01h	Rd	
	Product ID Low	8	02h	Rd	
	Product ID High	8	03h	Rd	
Digital audio interface configuration 1	-	8	04h	Rd/Wr	*Table 10*
Digital audio interface configuration 2	-	8	05h	Rd/Wr	*Table 11*
Data transfer mode	-	8	06h	Rd/Wr	*Table 12*
Audio mode	-	8	07h	Rd/Wr	*Table 13*
Line in left configuration	-	8	08h	Rd/Wr	*Table 14*
Line in right configuration	-	8	09h	Rd/Wr	*Table*
Headset output left configuration	-	8	0Ah	Rd/Wr	*Table 16*
Headset output right configuration	-	8	0Bh	Rd/Wr	*Table 17*
DAC left configuration	-	8	0Ch	Rd/Wr	*Table 18*
DAC right configuration	-	8	0Dh	Rd/Wr	*Table 19*
Line out left configuration	-	8	0Eh	Rd/Wr	*Table 20*
Line out right configuration	-	8	0Fh	Rd/Wr	*Table 21*
Interrupt polarity control	-	8	10h	Rd/Wr	*Table 22*
Interrupt open drain control	-	8	11h	Rd/Wr	*Table 23*
Interrupt mask control	-	8	12h	Rd/Wr	*Table 24*
Interrupt status	-	8	13h	Rd/Clear	*Table 25*
Chip status	-	8	14h	Rd	*Table 26*
Reserved	-	8	15h	-	
Balance configuration	-	8	16h	Rd/Wr	*Table 28*
Clock configuration register	-	8	17h	Rd/Wr	*Table 29*
Chip configuration	-	8	18h	Rd/Wr	*Table 30*
PSM configuration	-	8	19h	Rd/Wr	*Table 31*
SMAB configuration	-	8	1Ah	Rd/Wr	*Table 32*
Reserved	-	8	1Bh	-	

Table 8. Register map (continued)

Register set	Field name	Size (bits)	Register address (8 bits)	Access	Reference
Fade in	-	8	1Ch	Rd/Wr	*Table 34*
Reserved	-	8	1Dh -> FFh	-	

6.1 Register details

6.1.1 ID registers

Table 9. Chip ID (address: 00h-03h read-only)

Field name	Bits	Access	Reset	Description
Vendor ID Low	7:0	rd	83h	Lower byte of Vendor ID
Vendor ID High	7:0	rd	04h	Upper byte of Vendor ID
Product ID Low	7:0	rd	01h	Lower byte of Product ID
Product ID High	7:0	rd	11h	Upper byte of Product ID

6.1.2 Interface configuration registers

Table 10. Digital audio interface configuration 1 (address 04h)

Field name	Bits	Access	Default	Description
UNUSED	0	-	0	Reserved
DAMAST	6	rd/wr	0	Slave/master mode selection: 0: Slave 1: Master
DASYNC	5	rd/wr	0	DA_SYNC polarity inverting: 0: Falling edge of DA_SYNC starts a frame 1: Rising edge of DA_SYNC starts a frame
DACKP	4	rd/wr	0	DA_CK polarity inverting: 0: DA_SYNC and DA_CK falling edges are synchronous 1: DA_SYNC falling and DA_CK rising edges are synchronous
DACHSW	3	rd/wr	0	precedence of left and right channel relative to DA_SYNC active edge: 0: Left first 1: Right first
DAFORM	2:1	rd/wr	00	I²S format selection 00: Delayed 01: Left aligned 10: Right aligned 11: Delayed
ENDIAN	0	rd/wr	0	Endian selection: 0: MSB first 1: LSB first

Table 11. Digital audio interface configuration 2 (address 05h)

Field name	Bits	Access	Default	Description
UNUSED	7:6	-	00	Reserved for future use
I2CVR	5	rd/wr	0	I2C typical voltage range 0: 1.8V +/-10% 1: 3.3V +/-10%
FMFEN	4	rd/wr	1	I2C High speed filter enable 0: disable 1: enable (50ns spike suppression)

Table 11. Digital audio interface configuration 2 (address 05h) (continued)

Field name	Bits	Access	Default	Description
BDEPTH	3:2	rd/wr	01	Bit length in I²S format selection for each channel 00: 32 bits 01: 24 bits 10: 16 bits 11: 16 bits
FLENGTH	1:0	rd/wr	01	Data length selection 00: 2x32 bits 01: 2x24 bits 10: 2x16 bits 11: 2x16 bits

Table 12. Data transfer mode (address 06h)

Field name	Bits	Access	Default	Description
UNUSED	7	-	1	Reserved for future use
SUSPEND_N	6	rd/wr	0	Data transfer enable: 0: Data transfer disabled 1: Data transfer enabled
UNUSED	5:0	-	001000	Reserved for future use

Table 13. Audio mode (address 07h)

Field name	Bits	Access	Default	Description
SRATE	7:4	rd/wr	1001	Input sample rate: 0000: 8 kHz 0001: 11.025 kHz 0010: 12 kHz .. 0100: 16 kHz 0101: 22.05 kHz 0110: 24 kHz .. 1000: 32 kHz 1001: 44.1 kHz 1010: 48 kHz .. 1110: 96 kHz 1111: 192 kHz .. Other: 44.1 kHz
CLK_IN_FREQ	3:1	rd/wr	000	Master clock frequency input: 000: disabled 001 to 011: 32 kHz 100: 13 MHz 101: 19.2 MHz 110: 26 MHz 111: 38.4 MHz
PLL_BYPASS	0	rd/wr	0	PLL bypass: 0: PLL is used 1: PLL is bypassed and off

6.1.3 Gain configuration registers

Table 14. Line in left configuration (address 08h)

Field name	Bits	Access	Default	Description
LINGL	7:3	rd/wr	10101	Line In left Gain selection 00000: -42 dB 00001: -40 dB ..step 2 dB 10101: 0 dB .. 11111: +20 dB
UNUSED	2:0	rd/wr	010	Reserved for future use

Table 15. Line in right configuration (address 09h)

Field name	Bits	Access	Default	Description
LINGR	7:3	rd/wr	10101	Line In right gain selection 00000: -42 dB 00001: -40 dB ..step 2 dB 10101: 0 dB .. 11111: +20 dB
UNUSED	2:0	rd/wr	010	Reserved for future use

Table 16. Headset left output configuration (address 0Ah)

Field name	Bits	Access	Default	Description
HSGL	7:4	rd/wr	1011	Headset right gain selection 0000 to 0101: -18 dB 0110: -16dB ..step 2 dB 1011: -6dB .. 1111: +2 dB
UNUSED	3:0	rd/wr	0010	Reserved for future use

Table 17. Headset right output configuration (address 0Bh)

Field name	Bits	Access	Default	Description
HSGR	7:4	rd/wr	1011	Headset left gain selection 0000 to 0101: -18 dB 0110: -16dB ..step 2 dB 1011: -6dB .. 1111: +2 dB
UNUSED	3:0	rd/wr	0010	Reserved for future use

Table 18. DAC left configuration (address 0Ch)

Field name	Bits	Access	Default	Description
DACGL	7:2	rd/wr	111101	DAC left gain selection 000000: -62 dB 000001: -60.5 dB 000010: -59 dB ..step 1 dB 110111: -6dB .. 111101: 0 dB .. 111111: +2 dB
UNUSED	1:0	rd/wr	10	Reserved for future use

Table 19. DAC right configuration (address 0Dh)

Field name	Bits	Access	Default	Description
DACGR	7:2	rd/wr	111101	DAC right Gain selection 000000: -62 dB 000001: -60.5 dB 000010: -59 dB ..step 1 dB 110111: -6dB .. 111101: 0 dB .. 111111: +2 dB
UNUSED	1:0	rd/wr	10	Reserved for future use

Table 20. Line out left configuration (address 0Eh)

Field name	Bits	Access	Default	Description
LOUGL	7:4	rd/wr	1010	Line Out left Gain selection 0000: -30 dB 0001: -27 dB .. step 3 dB 1000: -6 dB .. 1010 to 1111: 0 dB
UNUSED	3:0	rd/wr	0010	Reserved for future use

Table 21. Line out right configuration (address 0Fh)

Field name	Bits	Access	Default	Description
LOUGR	7:4	rd/wr	1010	Line Out right Gain selection 0000: -30 dB 0001: -27 dB ..step 3 dB 1000: -6 dB .. 1010 to 1111: 0 dB
UNUSED	3:0	rd/wr	0010	Reserved for future use

6.1.4 Interrupt registers

Table 22. Interrupt polarity control (address 10h)

Field name	Bits	Access	Default	Description
HDETPOL	7	rd/wr	0	IRQ-HDET interrupt output polarity selection: 0: active low 1: active high
UNUSED	6:0	rd/wr	000000	Reserved for future use

Table 23. Interrupt open drain control (address 11h)

Field name	Bits	Access	Default	Description
HDETOD	7	rd/wr	0	IRQ_HDET pad open drain control: 0: open drain (active low) 1: CMOS (polarity defined in Interrupt polarity control register)
UNUSED	6:0	rd/wr	000000	Reserved for future use

Table 24. Interrupt mask control (address 12h)

Field name	Bits	Access	Default	Description
HDETENABLE	7	rd/wr	1	Headphone plug interrupt mask set: 0: interrupt is masked (but memorized) 1: interrupt is enabled (physical line is IRQ_HDET)
UNUSED	6	rd/wr	0	Reserved for future use
PSMENABLE	5	rd/wr	0	Pop Smooth Machine interrupt mask set: 0: interrupt is masked (but memorized) 1: interrupt is enabled (physical line is IRQ_HDET)
UNUSED	4:0	rd/wr	00000	Reserved for future use

Table 25. Interrupt status (address 13h)

Field name	Bits	Access	Default	Description
HDET	7	rd / clear	0	Headphone plug insertion is detected when “1” This bit is cleared after reading and it resets the IRQ_HDET interrupt line.
UNUSED	6	rd/wr	0	Reserved for future use
PSM_END	5	rd / clear	0	Pop Smooth Machine has finished when “1” This bit is cleared after reading and it resets the IRQ_HDET interrupt line.
UNUSED	4:0	rd	00000	Reserved for future use

6.1.5 Status registers

Table 26. Chip status (address 14h)

Field name	Bits	Access	Default	Description
UNUSED	7:5	-	000	Reserved for engineering.
HEADSET	4	rd	-	Headset connection: 0: Headset not connected 1: Headset connected
UNUSED	3:0	rd	0000	Reserved for future use

Table 27. Reserved (address 15h)

Field name	Bits	Access	Default	Description
UNUSED	7:0	-	-	Reserved for engineering

Table 28. Balance configuration (address 16h)

Field name	Bits	Access	Default	Description
DACB	7	rd/wr	0	DAC balance enable: 0: left channel gain setting is duplicated on right channel 1: both channels gain setting are independent
HSB	6	rd/wr	0	HS balance enable: 0: left channel gain setting is duplicated on right channel 1: both channels gain setting are independent
LINB	5	rd/wr	0	Line in balance enable: 0: left channel gain setting is duplicated on right channel 1: both channels gain setting are independent
LOUB	4	rd/wr	0	Line out balance enable: 0: left channel gain setting is duplicated on right channel 1: both channels gain setting are independent
UNUSED	3:0	rd/wr	0000	Reserved for future use

Table 29. Clock configuration register (address 17h)

Field name	Bits	Access	Default	Description
UNUSED	7:5	rd/wr	000	Reserved for future use
CLK_OUT_FREQ	4:2	rd/wr	000	Master clock output frequency: 000: 19.2 MHz 001: 38.4 MHz 010: 76.8 MHz 011: 19.2 MHz 100: 26 MHz 101: 52 MHz 110: 78 MHz 111: 26 MHz
CLK_OUT_ENA	1	rd/wr	0	Master clock generation enable 0: CLK_OUT is disabled 1: CLK_OUT is enabled, frequency is selected by CLK_OUT_FREQ[4:2]
UNUSED	0	rd/wr	0	Reserved for future use

Table 30. Chip configuration (address 18h)

Field name	Bits	Access	Default	Description
RESERVED	7:6	-	10	Reserved for future use
HS_LEVEL(1)	5	rd/wr	0	SMAB high level SMPS output voltage control: 0: 2.2V, allows 1Vrms output on HS with minimum battery voltage 2.5V 1: 1.8V, allows 0.8Vrms output on HS with minimum battery voltage 2.3V
DRESET_N	4	rd/wr	1	Digital reset: 0: digital section is in reset 1: digital section is active
SOFT_RESET(2)	3	rd/wr	0	Registers reset: all registers recover their default value. 0: normal behavior 1: all registers recover their default value
UNUSED	2:0	rd/wr	000	Reserved for future use

1. HS_LEVEL has an impact on power consumption, see *Table 50*
2. When “1” is written, all registers recover their default value, including this register. A new read on this bit will show “0”. It is not possible to read “1” on this bit

Table 31. PSM configuration (address 19h)

Field name	Bits	Access	Default	Description
UNUSED	7:4	rd/wr	0000	Reserved for future use
ISEL[(1)]	3:2	rd/wr	00	Input selection: 00: no input selected 01: Digital input selected 10: Line input selected 11: Both digital and line inputs selected
OSEL[(2)]	1:0	rd/wr	00	Output selection: 00: no output selected 01: Headphone output selected 10: Line output selected 11: Both headphone and line outputs selected

1. Writing this register will generate an interrupt when PSM has finished
2. Writing this register will generate an interrupt when PSM has finished

Note: Device Inputs (ISEL) and Outputs (OSEL) must be configured at the same time in this register, to generate only one interrupt when PSM has finished

Table 32. SMAB configuration (address 1Ah)

Field name	Bits	Access	Default	Description
SMAB_ENABLE	7	rd/wr	0	SMAB enable: 0: disabled 1: enabled
SMAB_THRESHOLD	6:0	rd/wr	0100000	Signal level detection for SMAB supply threshold: 0000000: supply switch from low to high when digital input is higher than 2^{BDEPTH} x0%, means supply is always at high level 0000001: supply switch from low to high when digital input is higher than 2^{BDEPTH} x 1% ..step 1% 0100000: supply switch from low to high when digital input is higher than 2^{BDEPTH} x 32% .. 0110010: supply switch from low to high when digital input is higher than 2^{BDEPTH} x 50% .. 1100100 to 1111111: supply switch from low to high when digital input is higher than 2^{BDEPTH} x 100%, means supply is always at low level

Table 33. Reserved (address 1Bh)

Field name	Bits	Access	Default	Description
UNUSED	7:0	-	-	Reserved for future use

Table 34. Fade in (address 1Ch)

Field name	Bits	Access	Default	Description
FADE_BYPASS	7	rd/wr	0	Anti-click activation(1): 0: active 1: not active
FADE_DELAY	6:4	rd/wr	011	Delay between each gain change(2): 000: 46µs for DAC, 30µs for line in and line out 001: 92µs for DAC, 61µs for line in and line out 010: 184µs for DAC, 122µs for line in and line out 011: 369µs for DAC, 244µs for line in and line out 100: 738µs for DAC, 488µs for line in and line out 101: 1.48ms for DAC, 977µs for line in and line out 110: 2.95ms for DAC, 1.95ms for line in and line out 111: 5.9ms for DAC, 3.91ms for line in and line out
UNUSED	3:0	rd/wr	0000	Reserved for future use

1. Fade out cannot be bypassed when audio path is powered down through PSM register
2. Delay for both fade in and fade out. Timing given for DAC can vary from +/-15% depending on clock input frequency. Minimum delay must be programmed if fade out is not needed

Table 35. Reserved (address 1Dh => FFh)

Field name	Bits	Access	Default	Description
UNUSED	7:0	-	-	Reserved for engineering

7 General electrical requirements

7.1 Absolute maximum ratings

Caution: “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36. Absolute maximum ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
	V_{BAT} to GND	-0.5	-	6	V
	V_{IO} to GND	-0.5	-	6	V
	Storage temperature range	-40	-	125	°C
	ESD HBM (human body model) Standard: JESD22-A114	-1	-	+1	kV
	ESD CDM (charged device model) Standard: JESD22-C101	-500	-	+500	V

7.2 Operating conditions

Table 37. Qualified DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Operating temperature range	-30	-	85	°C
V_{BAT}	Positive supply	2.3	-	4.8	V
V_{IO}	IO voltage	1.62	-	3.6	V

8 Electrical characteristics

Unless otherwise specified, V_{BAT} = 3.6 V, V_{IO} = 1.8 V, T_{AMB} = 25 °C; signal frequency = 1kHz, channel gain = 0dB, sample rate = 44.1kHz; all signals are referenced to GND, 32 kHz clock jitter < 300 ppm. All signals measured at the chip pin level with RS_{HS}=12 Ω and CP_{HS}=3.3 nF (see *Table 16*). SMAB™ on

8.1 Interface

8.1.1 Digital interface

Table 38. Digital interface

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	-	-0.3	-	0.35 x VIO	V
V_{IH}	Input high voltage	-	0.65 x VIO	-	VIO + 0.3	V
I_{IL}	Low level input current	-	-1.0	-	1.0	µA
I_{Ih}	High level input current	-	-1.0	-	1.0	µA
V_{OL}	Output low voltage	Output sink current 4 mA	-	-	0.3	V
V_{OH}	Output high voltage	Output source current 4 mA	VIO - 0.3	-	-	V
C_{OD}	Capacitive load on output pads	-	-	50	-	pF
C_{IN}	Input capacitance	-	-	-	10	pF
V_{OD}	Open drain output low voltage	Output sink current 4 mA	0	-	0.3	V
$I2C_{PU}$	Pull-up resistance on I2C bus	10pF < Cbus < 100pF	2300		2700	Ω
		100pF < Cbus < 400pF	600		800	Ω
Tr_{IRQ}	IRQ rise time	Capacitive load = C_L	2+0.3 x C_L		3+0.4 x C_L	ns

8.1.2 Analog interface

Figure 16. Load model

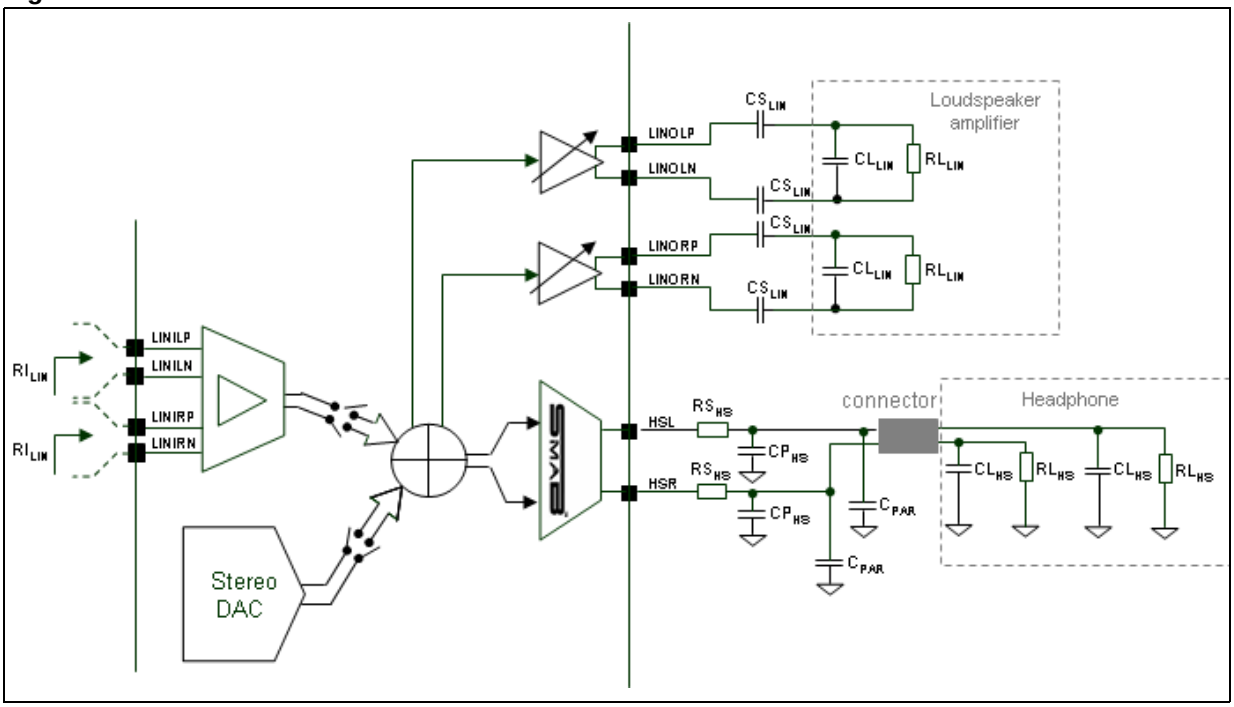


Table 39. Analog interface

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RI_{LIN}	Line in input resistance	differential	20(1)	-	250(2)	kΩ
RL_{HS}	HS drivers load resistance	HS to GND single ended	16	32	-	Ω
$CL_{HS}+C_{PAR}+CP_{HS}$	HS drivers total load capacitance	RS_{HS}=12 Ω, RL_{HS}=16 Ω	2.5		5	nF
		RS_{HS}=12 Ω, RL_{HS}=10 kΩ	2.5		100	nF
RL_{LIN}	Line out drivers load resistance	In differential, CS_{LIN}=1 µF	10	-	-	kΩ
CL_{LIN}	Line out drivers load capacitance	-	-	-	200	pF
HD_{RES}	External resistance from plug to ground for plug detection	-	-	-	10	Ω
HD_{DEB}	Headset plug-in detection debounce time		-	30	-	ms

1. Line in gain dependant
2. Line in gain dependant

8.2 Power management

The AV5205 is self powered from battery thanks to 2 low drop-out voltage regulators and one negative charge pump. These power management sources cannot be used to supply external devices.

Table 40. Power management

Parameter	Conditions	Min.	Typ.	Max.	Unit
LDO's VDIG, VANA and VPLL supply range		2.3	-	4.8	V
LDO VANA output voltage		1.94	2	2.06	V
LDO VDIG output voltage		1.16	1.2	1.24	V
LDO VPLL output voltage		1.74	1.8	1.85	V
SMPS supply range		2.3	-	4.8	V
SMPS output voltage	external components described in *Table*	1.14	-	2.31	V
SMPS output current	external components described in *Table*	-	-	160	mA
SMPS power efficiency	5mVrms audio signal external components described in *Table*	-	82	-	%
SMPS frequency	HS drivers enabled, current from 0 to 160mA external components described in *Table*	25		1760	kHz
Negative Charge pump supply range		1.14	-	2.31	V
Negative Charge pump output voltage	external components described in *Table*	-2.3	-	-0.8	V
Charge pump frequency	HS drivers enabled, current from 0 to 120mA external components described in *Table*	45	800	880	kHz

8.3 Audio specifications

Table 41. DAC to HS specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HS_{LVL}	DAC to HS output reference	Analog sinusoid output voltage obtained at HS driver output with a full-scale digital input word and all gains in the path set to 0 dB without load				
		With or without load , HS_LEVEL=0	-	0 1 2.82	-	dBVrms Vrms Vpp
		With or without load , HS_LEVEL=1	-	-1.94 0.8 2.26	-	dBVrms Vrms Vpp
	Digital gain range	-	-62	-	+2	dB
	Digital gain step	-	-	1(1)		dB
	Analog gain range	-	-18	-	+2	dB
	Analog gain step	-	-	2		dB
	Total channel gain error	Any gain	-0.6		+0.6	dB
	Analog gain mismatch	L to R	-0.2	-	+0.2	dB
DR	Dynamic range(2)	RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF, Aweighted,, 0 dBFS input signal				
		HS_LEVEL=0 gain 0 dB	98	102	-	dB
		HS_LEVEL=1 gain -2 dB	97	100	-	dB
THD+N	THD plus noise	RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF, Aweighted, gain 0 dB, input signal at -10dBFS				
		HS_LEVEL=0	75	78	-	dB
		HS_LEVEL=1	75	78	-	dB
SNR	Signal to noise ratio(3)	RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF, Aweighted, gain -2 dB, 0 dBFS input signal				
		HS_LEVEL=0	99	102	-	dB
		HS_LEVEL=1	97	100	-	dB
EN	Integrated noise in [20 Hz, 20 kHz] band	RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF, Aweighted				
		HS gain = +2dB	-	8.9	12.6	µVrms
		HS gain = 0dB	-	7.9	11.2	µVrms
		HS gain = -6dB	-	5.7	8.1	µVrms
		HS gain = -12dB	-	4.5	6.3	µVrms
		HS gain = -18dB	-	3.7	5.3	µVrms

Table 41. DAC to HS specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HS_{THD}	Total harmonic distortion	RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF, 1 kHz, 0dB gain, **HS_LEVEL=0**				
		HS out = -2dBVrms		0.013		%
		HS out = -6dBVrms		0.013		%
		HS out = -20dBVrms		0.013		%
		RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF, 1 kHz, 0dB gain, **HS_LEVEL=1**				
		HS out = -4dBVrms		0.013		%
		HS out = -20dBVrms		0.013		%
	Common mode voltage	-	-	0	-	V
	Offset	Gain 0dB	-0.8	-	+0.8	mV
	Crosstalk between left and right channel	Without load	-	-86	-80	dB
PSR_{HS}	Power supply rejection	0.5 Vpp signal @3.6 V on VBAT				
		1 kHz 5 kHz 20 kHz	-	100 90 80	-	dB
		0.2 Vpp signal @2.4 V on VBAT				
		1 kHz 5 kHz 20 kHz	95 85 75	-	-	dB

1. 2 first steps are 1.5dB: -62dB to -60.5dB and -60.5dB to -59dB
2. THD + noise in [20 Hz; 20 kHz] band, measured at -60 dBFS adding 60 dB, Aweighted, SMAB_LEVEL=0
3. Ratio between HS_{LVL} and integrated noise floor Aweighted adding 60 dB, SMAB_LEVEL=0

Table 42. DAC to Line out specification

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$LOUTdif_{LVL}$	DAC to line out differential output reference	Analog sinusoid output voltage obtained at line out driver output in **differential mode** with a full scale digital input word an all gains in the path set to 0 dB	-	0 1 2.82	-	dBVrms Vrms Vpp diff
$LOUTse_{LVL}$	DAC to line out single ended output reference	Analog sinusoid output voltage obtained at line out driver output in **single ended mode** with a full scale digital input word an all gains in the path set to 0 dB	-	-6 0.5 1.41	-	dBVrms Vrms Vpp
	Digital gain range	-	-62	-	+2	dB
	Digital gain step	-	-	1	-	dB

Table 42. DAC to Line out specification (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Analog gain range	-	-30	-	0	dB
	Analog gain step	-	-	3	-	dB
	Total channel gain error	Any gain	-0.6		+0.6	dB
	Analog gain mismatch	L to R	-0.2	-	+0.2	dB
DR	Dynamic range(1)	RL_{LIN}=10 kΩ, gain 0 dB				
		Differential mode	99	101	-	dB
		Single ended mode	TBD	TBD	-	dB
SNR	Signal to noise ratio(2)	RL_{LIN}=10 kΩ, gain 0 dB				
		Differential mode	99	101	-	dB
		Single ended mode	89	92	-	dB
EN	Integrated noise in [20 Hz, 20 kHz] band	RL_{LIN}=10 kΩ, gain 0 dB				
		Differential mode	-	9	11.2	µVrms
		Single ended mode	-	12.8	17.8	µVrms
LIN_{THD}	Total harmonic distortion	**Differential mode**, 1 kHz, RL_{LIN}=10 kΩ 0dB gain				
		Line Out = -2dBVrms	-	0.01		%
		Line Out = -6dBVrms	-	TBD		%
		Line Out = -20dBVrms	-	TBD		%
		Single ended mode, 1 kHz, RL_{LIN}=5 kΩ 0dB gain				
		Line Out = -8dBVrms	-	0.01		%
		Line Out = -20dBVrms	-	TBD		%
	Common mode voltage		-	0.95	-	V
	Crosstalk between left and right channel	RL_{LIN}=10 KΩ	-	-85	-70	dB
PSR_{LO}	Power supply rejection	1 kHz, 0.5 V pp signal @3.6 V on VBAT				
		Differential mode	-	90	-	dB
		Single ended mode	-	80	-	dB
		1 kHz, 0.2 V pp signal @2.4 V on VBAT				
		Differential mode	85	-	-	dB
		Single ended mode	75	-	-	dB

1. THD + noise in [20 Hz; 20 kHz] band, measured at -60 dBFS adding 60 dB, Aweighted
2. Ratio between LIN_{LVL} and integrated noise floor Aweighted adding 60 dB

Table 43. Line in to HS specification

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$LINdif_{LVL}$	Line in differential to HS output reference	Analog sinusoid output voltage obtained at HS driver output with 1 Vrms at line in input in **differential mode** and all gains in the path set to 0 dB	-	0 1 2.82	-	dBVrms Vrms Vpp
$LINse_{LVL}$	Line in single ended to HS output reference	Analog sinusoid output voltage obtained at HS driver output with 0.5 Vrms at line in input in **single ended mode** and all gains in the path set to 0 dB	-	-6 0.5 1.41	-	dBVrms Vrms Vpp
	Line in gain range	-	-42	-	+20	dB
	Line in gain step	-	1.8	2	2.2	dB
	Left / right gain matching	-	-0.2	-	0.2	dB
	HS driver gain range	-	-18	-	+2	dB
	HS driver gain step	-	-	2	-	dB
	Total channel gain error	Any gain	-0.6		+0.6	dB
	Input level	Differential mode		1		Vrms
		Single ended mode		0.5		Vrms
DR	Dynamic range(1)	**Differential mode, Line in gain 0 dB**, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF				
		HS_LEVEL=0	95	98	-	dB
		HS_LEVEL=1	93	96	-	dB
		Single ended, Line in gain +6 dB, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF				
		HS_LEVEL=0	88	90	-	dB
		HS_LEVEL=1	86	88	-	dB
SNR	Signal to noise ratio(2)	**Differential mode, Line in gain 0 dB**, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF				
		HS_LEVEL=0	95	98	-	dB
		HS_LEVEL=1	93	96	-	dB
		Single ended, Line in gain +6 dB, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF				
		HS_LEVEL=0	90	93	-	dB
		HS_LEVEL=1	88	91	-	dB

Table 43. Line in to HS specification (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EN	Integrated noise in [20 Hz, 20 kHz] band	**Differential mode, Line in gain 0 dB**, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF				
		HS gain +2 dB	-	16	23	µVrms
		HS gain 0 dB	-	12	17	µVrms
		HS gain -6 dB	-	9	13	µVrms
		HS gain -12 dB	-	7	10	µVrms
		HS gain -18 dB	-	7	10	µVrms
		Single ended mode, Line in gain +6 dB, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF				
		HS gain +2 dB	-	29	41	µVrms
		HS gain 0 dB	-	22	31	µVrms
		HS gain -6 dB	-	17	23	µVrms
		HS gain -12 dB	-	13	18	µVrms
		HS gain -18 dB	-	13	18	µVrms
HS_{THD}	Total harmonic distortion	**Differential mode, Line in gain 0 dB**, HS gain 0 dB, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF **HS_LEVEL = 0**				
		HS out = -2dBVrms	-	0.013	-	%
		HS out = -6dBVrms	-	TBD	-	%
		HS out = -20dBVrms	-	TBD	-	%
		Differential mode, Line in gain 0 dB, HS gain 0 dB, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF **HS_LEVEL = 1**				
		HS out = -4dBVrms	-	0.013	-	%
		HS out = -20dBVrms	-	TBD	-	%
		Single ended mode, **Line in gain +6 dB**, HS gain 0 dB, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF **HS_LEVEL = 0**				
		HS out = -2dBVrms	-	0.03	-	%
		HS out = -6dBVrms	-	TBD	-	%
		HS out = -20dBVrms	-	TBD	-	%
		Single ended mode, **Line in gain +6 dB**, HS gain 0 dB, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF **HS_LEVEL = 1**				
		HS out = -4dBVrms	-	0.03	-	%
		HS out = -20dBVrms	-	TBD	-	%
	Common mode voltage	-	-	0	-	V
	Offset	Gain 0dB	-0.8	-	+0.8	mV

Table 43. Line in to HS specification (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Crosstalk between left and right channel	Without load	-	-86	-80	dB
PSR_{HS}	Power supply rejection	0.5 Vpp signal @3.6 V on VBAT				
		1 kHz 5 kHz 20 kHz	-	90 80 70	-	dB
		0.2 Vpp signal @2.4 V on VBAT				
		1 kHz 5 kHz 20 kHz	85 75 65	-	-	dB

1. THD + noise in [20 Hz; 20 kHz] band, measured at 2.8mVpp differential at line in adding 60 dB, Aweighted, SMAB_LEVEL=0
2. Ratio between HS_{LVL} and integrated noise floor Aweighted adding 60 dB, SMAB_LEVEL=0

Table 44. Line in to Line out specification

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$LINOUTdif_{LVL}$	Line in differential to line out differential output reference	Analog sinusoid output voltage obtained at line out driver output in **differential mode** with 1Vrms at line in input in **differential mode** and all gains in the path set to 0 dB	-	0 1 2.82	-	dBVrms Vrms Vppdiff
$LINOUTse_{LVL}$	Line in single ended to line out single ended output reference	Analog sinusoid output voltage obtained at line out driver output in **single ended mode** with 1Vrms at line in input in **single ended mode** and all gains in the path set to 0 dB	-	-12 0.25 0.71	-	dBVrms Vrms Vpp
	Line in gain range	-	-42	-	+20	dB
	Line in gain step	-	-	2	-	dB
	Line out gain range	-	-29	-	+1	dB
	Line out gain step	-	-	3	-	dB
	Total gain error	any gain	-0.6	-	+0.6	dB
	Left / right gain matching	-	-0.2	-	0.2	dB
	Input level	Differential mode	-	1	-	Vrms
		Single ended mode	-	0.5	-	Vrms

Table 44. Line in to Line out specification (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
LIN_{ML}	Output level	RL_{LIN}=10 kΩ, Line out differential, Line out gain 0 dB				
		Lin in Differential mode Line in gain 0 dB	-	1	-	Vrms
		Line in Single ended mode, Line in gain +6 dB	-	1	-	Vrms
DR	Dynamic range(1)	RL_{LIN}=10 kΩ, gain 0 dB differential mode on Line in and Line out	92	95	-	dB
SNR	Signal to noise ratio(2)	RL_{LIN}=10 kΩ, gain 0 dB differential mode on Line in and Line out	92	95	-	dB
EN	Integrated noise in [20 Hz, 20 kHz] band	output load =10 kΩ, Aweighted, gain 0 dB differential mode on Line in and Line out	-	18	25	µVrms
LIN_{THD}	Total harmonic distortion	1 kHz, LIN_{LVL}=1Vrms, RL_{LIN}=10 kΩ, gain 0 dB differential mode on Line in and Line out	-	0.05	-	%
	Common mode voltage	-	-	0.95	-	V
	Crosstalk	RL_{LIN}=10 kΩ LIN_{LVL}=2.9 dBVrms, gain 0 dB	-	-90	-70	dB
PSR_{LO}	Power supply rejection	1 kHz, 0.5 Vpp signal @3.6 V on VBAT	90	100	-	dB

1. THD + noise in [20 Hz; 20 kHz] band, measured at 2.8 mVpp differential at line in adding 60 dB, Aweighted
2. Ratio between LIN_{ML} and integrated noise floor Aweighted

Table 45. Digital filters specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Pass band	-	-	0.45 x Fs	-	-
	Stop band	-	-	0.54 x Fs	-	-
	Pass band ripple	-	-0.5	-	0	dB
	Out of band attenuation	-	95	-	-	dB
	Attenuation at 0.5 x Fs	-	15	-	-	dB
	Latency	From I²S to HS output	-	690	-	µs

Table 46. 32 kHz input clock signal specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Duty cycle	-	40	-	60	%
	Input frequency tolerance	@ 25 °C	-30	-	+30	ppm
	Input frequency variation temperature included	From -30 °C to 85 °C	32758.2 (-300 ppm)	32768	32777.8 (+300 ppm)	Hz
	Input jitter without SNR downgrading	Short term jitter from 2 up to 2000 cycles	-	-	1000	ppm

Figure 17. DAC to HS path dynamic range versus 32 kHz input jitter

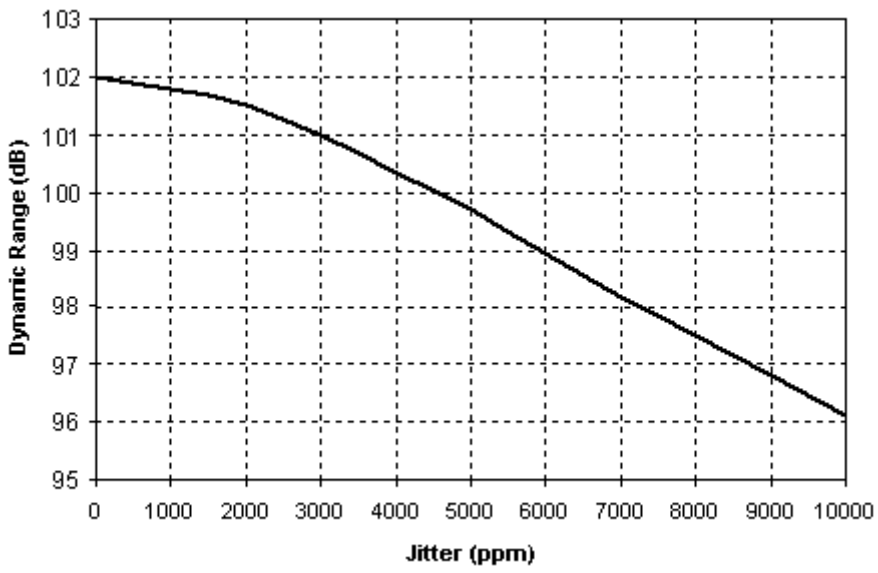


Table 47. CLK_OUT output specification

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Load capacitance	PCB parasitic capacitance on CLK_OUT pin			20	pF
	Duty cycle	-	45		55	%
	Output frequency	CLK_OUT_FREQ[2:0] = 000 001 010 100 101 110		 19.2 38.4 76.8 25.999 51.997 77.996		MHz
	Output frequency variation temperature included	From -30 °C to 85 °C	related to 32 kHz variation			Hz

Table 47. CLK_OUT output specification (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Output jitter	in [10 kHz:3 MHz] band		30		ps
	Power consumption	PLL consumption with CLK_OUT_ENA = 0		0.5		mA
		PLL consumption with 20 pF load on pad: CLK_OUT_FREQ[2:0] = x00 x01 x10 x11		 1.4 2.3 2.9 4.1		mA

Table 48. Digital interface Clock frequencies in I²S master mode

CLK_IN frequency	PLL	CLK_OUT frequency (MHz)	DA_SYNC frequency (kHz)	deviation from exact sample rate (ppm)
32 kHz	ON	19.2	8.000, 16.000, 32000 11.034; 22.069, 44.138 12.030, 24.060, 48.120 96.241, 192.481	0 +3136 +2500 +2505
		38.4		
		76.8		
		25.999	8.005, 16.010, 32.020 11.016, 22.033, 44.066 12.036, 24.073, 48.146 96.291, 192.583	+625 +1500 +3042 +3036
		51.997		
		77.996		
13 MHz or 26 MHz	ON	N.A.	8.005, 16.010, 32.020 11.017, 22.034, 44.068 12.037, 24.074, 48.148, 96.296, 192.593	+625 +1545 +3083 +3089
19.2 MHz or 38.4 MHz	ON	N.A.	8.005, 16.011, 32.021 11.018, 22.035, 44.070 12.038, 24.075, 48.151, 96.301, 192.603	+656 +1591 +3146 +3141
26 MHz	OFF	N.A.	8.000, 16.000, 32.000 11.009, 22.018, 44.034, 12.000, 24.000, 48.000, 96.000, 192.000	+0 +773 +0 +0
19.2 MHz(1) or 38.4 MHz	OFF	N.A.	8.005, 16.010, 32.020 11.017, 22.034, 44.068 12.037, 24.074, 48.148, 96.296, 192.593	+625 +1545 +3083 +3089

1. If CLK_IN = 19.2 MHz PLL must be on to support 192kHz sampling rate

8.4 Power consumption

8.4.1 Power consumption tables for all the paths

Characteristics are specified at V_{BAT} = 3.6 V, V_{IO} = 1.8V, T_{AMB} = 25°C, CLK_OUT_ENA=0, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF

Table 49. Current consumption with silent audio signal

Parameter	Conditions		V_{BAT}	V_{IO}	Unit
Stand-by current	Default state		500	200	nA
Power consumption DAC to HS CLK_IN = 26 MHz, PLL off 44.1 kHz or 48 kHz sample rate	HS_LEVEL= 0(1)	SMAB 50%	2.9	1.5	mA
		SMAB off	3.7	1.5	
	HS_LEVEL = 1(2)	SMAB 50%	2.9	1.5	
		SMAB off	3.5	1.5	
Power consumption DAC to HS CLK_IN frequency = 32 kHz, PLL on, CLK_OUT off 44.1 kHz or 48 kHz sample rate	HS_LEVEL= 0	SMAB 50%	3.4	1.5	
		SMAB off	4.2	1.5	
	HS_LEVEL = 1	SMAB 50%	3.4	1.5	
		SMAB off	4	1.5	
Power consumption DAC to Line out, CLK_IN = 26 MHz, PLL off 44.1 kHz or 48 kHz sample rate	-		2.8	1. 7	
Power consumption DAC to Line out CLK_IN frequency = 32 kHz, PLL on, CLK_OUT off			3.4	1.7	
Power consumption in analog mode, Line in to HS, CLK_IN = 26 MHz, PLL off	HS_LEVEL= 0		3.2	0.08	
	HS_LEVEL = 1		3	0.08	
Power consumption in analog mode, Line in to HS, CLK_IN = 32 kHz, PLL on	HS_LEVEL= 0		4.7	0.001	
	HS_LEVEL = 1		4.5	0.001	
Power consumption in analog mode, Line in to Line out	-		2.4	0.001	

1. Maximum headphone output level = 1 Vrms
2. Maximum headphone output level = 0.8 Vrms

Table 50. Power consumption with 1 kHz sine wave in 2 x 32 ohm load

Parameter	Output signal level	Conditions		Power on VBAT	Power on VIO	Unit
Power consumption DAC to HS CLK_IN = 26 MHz, PLL off 44.1 kHz or 48 kHz sample rate	5mVrms	HS_LEVEL = 0[1]	SMAB 50%	10.4	3.8	mW
			SMAB off	13.1		
		HS_LEVEL = 1[2]	SMAB 50%	10.4		
			SMAB off	12.2		
	50mVrms	HS_LEVEL = 0	SMAB 50%	12.6	3.9	
			SMAB off	16.9		
		HS_LEVEL = 1	SMAB 50%	12.6		
			SMAB off	15.5		
	100mVrms	HS_LEVEL = 0	SMAB 50%	17.7	4.0	
			SMAB off	24		
		HS_LEVEL = 1	SMAB 50%	17.7		
			SMAB off	21.8		
	300mVrms	HS_LEVEL = 0	SMAB 50%	27.1	4.1	
			SMAB off	41.5		
		HS_LEVEL = 1	SMAB 50%	27.1		
			SMAB off	36.2		
Power consumption DAC to HS CLK_IN frequency = 32 kHz, PLL on, CLK_OUT off 44.1 kHz or 48 kHz sample rate	5mVrms	HS_LEVEL = 0	SMAB 50%	12.4	3.8	
			SMAB off	15		
		HS_LEVEL = 1	SMAB 50%	12.4		
			SMAB off	14.2		
	50mVrms	HS_LEVEL = 0	SMAB 50%	14.6	3.9	
			SMAB off	18.8		
		HS_LEVEL = 1	SMAB 50%	14.6		
			SMAB off	17.5		
	100mVrms	HS_LEVEL = 0	SMAB 50%	17.5	4.0	
			SMAB off	23.8		
		HS_LEVEL = 1	SMAB 50%	17.5		
			SMAB off	21.6		
	300mVrms	HS_LEVEL = 0	SMAB 50%	29.2	4.1	
			SMAB off	43.6		
		HS_LEVEL = 1	SMAB 50%	29.2		
			SMAB off	38.6		

1. Maximum headphone output level = 1 Vrms
2. Maximum headphone output level = 0.8Vrms

8.4.2 Power consumption curves

Curves are specified at V_{BAT} = 3.6 V, V_{IO} = 1.8V, T_{AMB} = 25°C, CLK_OUT_ENA=0, DAC to HS, CLK_IN = 26 MHz, PLL off, 44.1 kHz or 48 kHz sample rate, RL_{HS}=32 Ω, RS_{HS}=12 Ω, CP_{HS}=3.3 nF

Figure 18. DAC to HS power consumption with 1 kHz sine wave, HSLEVEL = 0

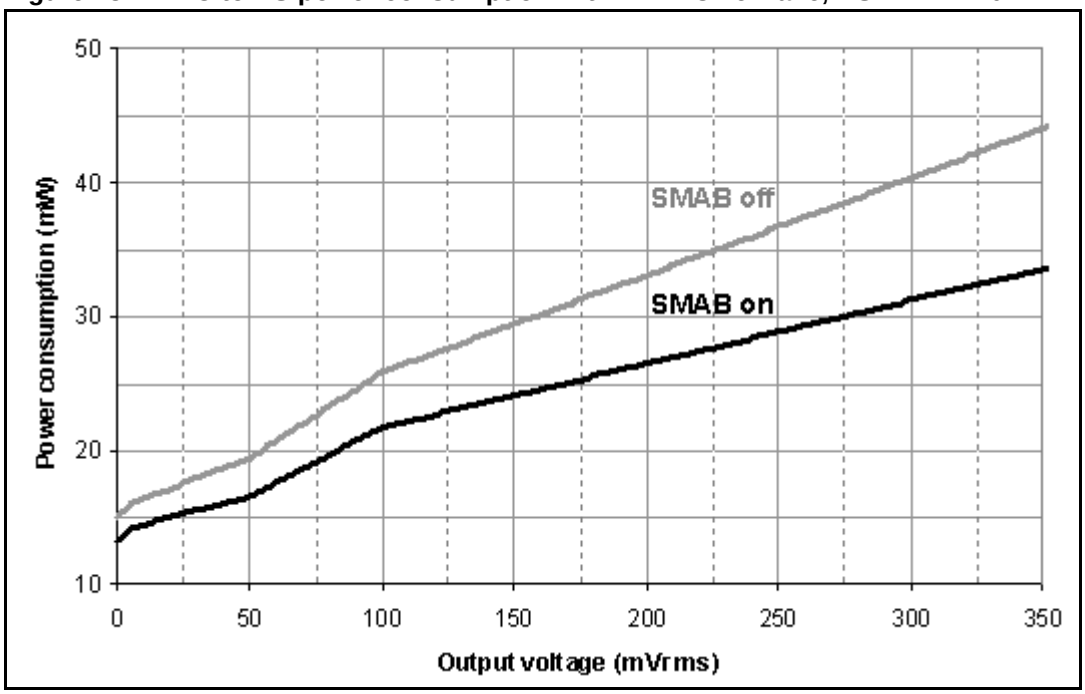
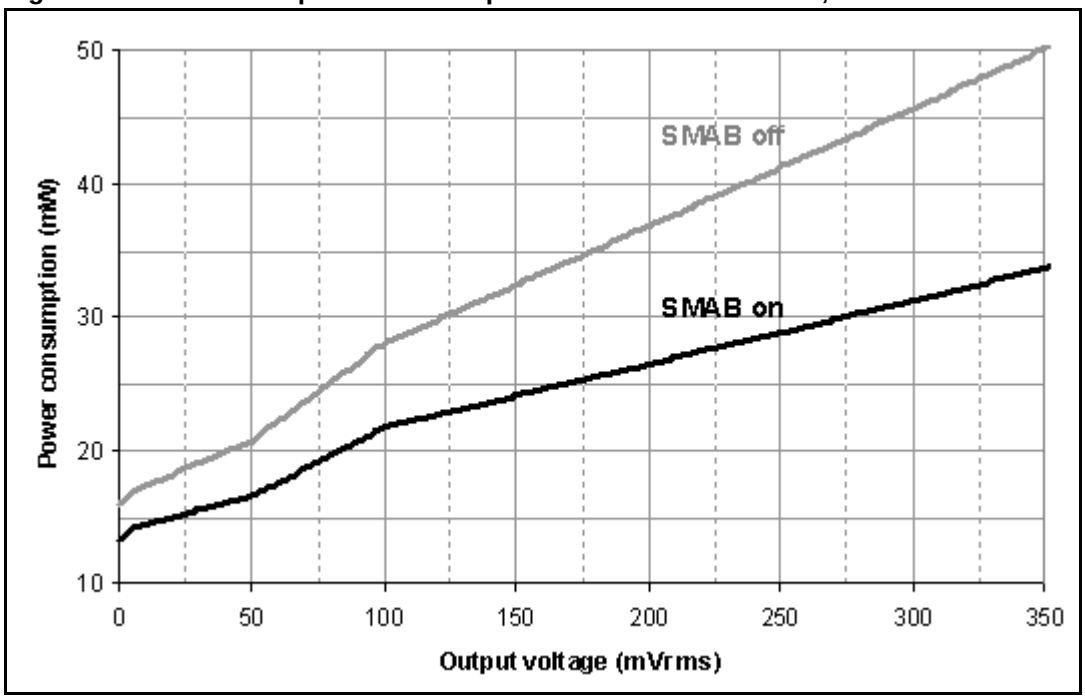


Figure 19. DAC to HS power consumption with 1 kHz sine wave, HSLEVEL = 1



9 Package mechanical data

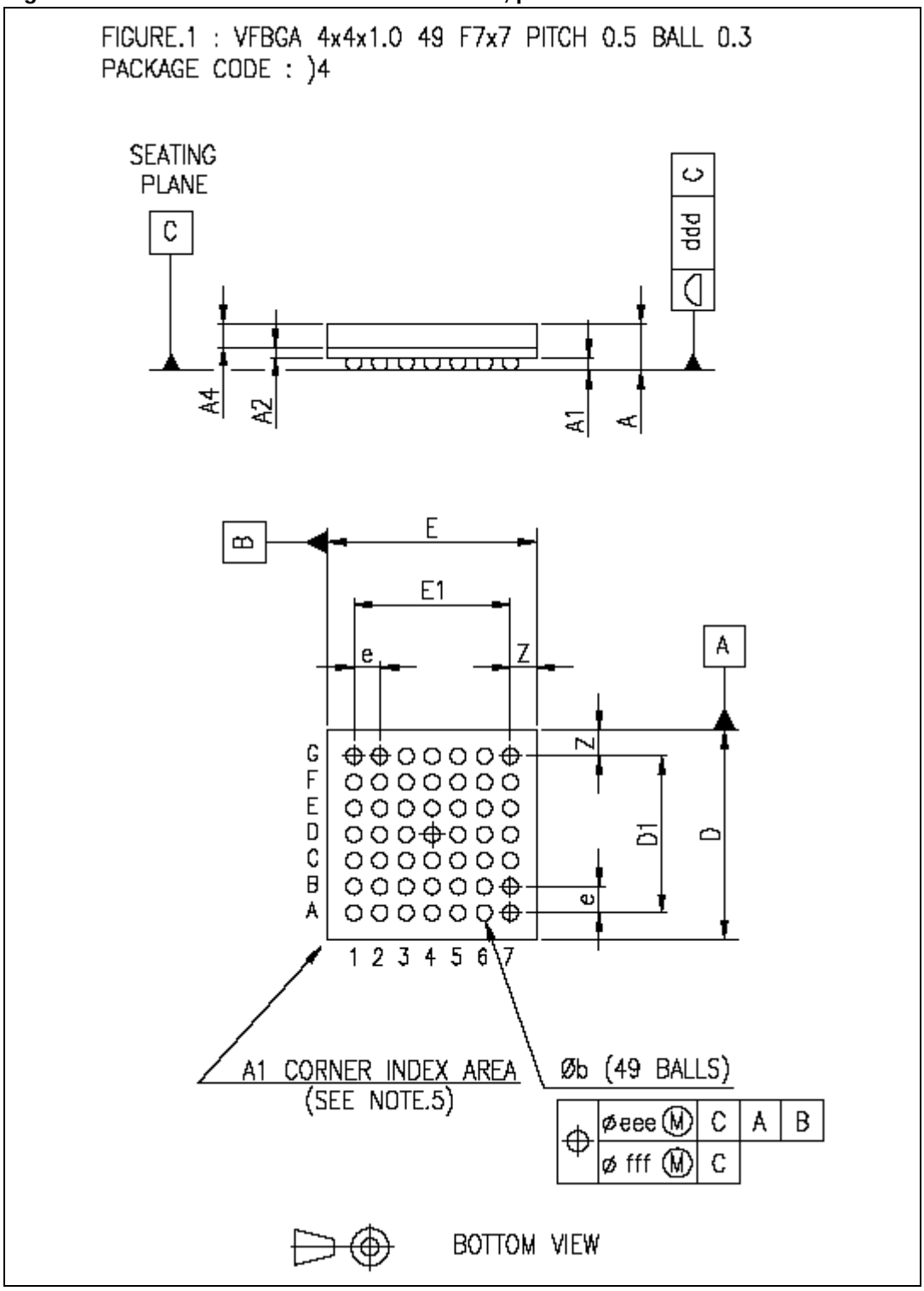
9.1 VFBGA49 4 mm x 4 mm x 0.91 mm

Table 51. VFBGA49 4 mm x 4 mm x0.91 mm, pitch 0.5 dimensions

Reference	DATABOOK			DRAWING			Notes
	Min.	Typ.	Max.	Min.	Typ.	Max.	
A			1.00			0.91	(1)
A1	0.15			0.16	0.21	0.26	
A2		0.20		0.16	0.20	0.24	
A4		0.435		0.42	0.435	0.45	
b	0.25	0.30	0.35	0.25	0.30	0.35	(2)
D	3.85	4.00	4.15	3.92	4.00	4.08	
D1		3.00			3.00		
E	3.85	4.00	4.15	3.92	4.00	4.08	
E1		3.00			3.00		
e		0.50			0.50		
F		0.50			0.50		
ddd			0.08			0.08	
eee			0.15			0.15	(3)
fff			0.05			0.05	(4)

1. - VFBGA stands for **V**ery thin Profile **F**ine Pitch **B**all **G**rid **A**rray.
   - Thin Profile: The total profile height (Dim A) is measured from the seating plane to the top of the component.
   - Thin profile: 0.80 < A < 1.00mm, Fine pitch: e < 1.00mm pitch
   - The maximum total package height is calculated by the following methodology: A1 Typ+A2 Typ+ A4 Typ + $(A1^2 + A2^2 + A4^2 \text{ tolerance values})^{1/2}$
2. The typical ball diameter before mounting is 0.30mm
3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 20. VFBGA49 4 mm x 4 mm x 0.91 mm, pitch 0.5 view



10 Ordering information

Table 52. Order codes

Part number	Package	Packing
AV5205C)4	VFBGA49 4 mm x 4 mm x 0.91mm, pitch 0.5 mm	Tray
AV5205C)4T	VFBGA49 4 mm x 4 mm x 0.91mm, pitch 0.5 mm	Tape and reel

11 Revision history

Table 53. Document revision history

Date	Revision	Changes
13-Apr-2011	1	Initial release.

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